

EFFECTS OF AC SYSTEM FREQUENCY SPECTRUM
ON COMMUTATION FAILURES
IN HVDC INVERTERS

By

GUDLEIFUR MARIS KRISTMUNDSSON

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To
my mother and father

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Various types of system disturbances will lead to commutation failure in hvdc (high voltage direct current) inverters, especially those connected to weak ac (alternating current) systems. This study analyzes the problem in terms of the frequency spectrum of the ac network.

A leading cause of commutation failure comes from the occurrence of a severe fault in the ac network. The transient response and the frequency spectrum of the ac system are important factors in determining the likelihood of commutation failure during a fault. The ac network typically has a low frequency dominant mode of oscillation in the 150-200 Hz range. This study shows that it is possible to increase the commutation volt-seconds and reduce the risk of failure, by increasing the frequency of the dominant oscillatory response of the network. Since the dominant frequency is sensitive to the size of the capacitor bank at the inverter bus, one possibility is to replace it with a new "filter," which provides the same fundamental VARs but shifts the frequency spectrum.

In order to evaluate the benefits of modifying the network spectrum for a variety of conditions, a computer simulation was set up for an hvdc system, using EMTP (Electro-

Magnetic Transients Program). A 12-pulse inverter is modeled in detail and is connected to a typical three-phase ac network model. The simulation model allows for study of commutation failures due to various types of faults which suppress the inverter bus voltage between 30–40%, with effective short circuit ratio ranging from 2.0–3.0 at the inverter bus.

Commutation failure is a statistical phenomenon which depends on random events, such as the time of occurrence of the fault. Thus, to get a measure of the probability of failure, multiple simulations were performed, as the time of fault was varied relative to the gating pulses at the inverter. Comparisons were made between the use of a straight capacitor bank and the new filter to increase the low-frequency resonance. Some results showed a complete elimination of commutation failures with the new filter, whereas in other cases the likelihood of failure was reduced dramatically.

CHAPTER 1

OVERVIEW OF HVDC SYSTEMS AND RESEARCH OBJECTIVES

Introduction

Early efforts in the practical use of electricity, both in telegraphy and in power and lighting, began with direct current. The first central electric power station in the world began operation in New York City in 1882. It delivered direct current to an area of just over 3 square miles at 110 V generated by Edison bipolar dc generators. Soon, many other large cities around the world started operation of similar power stations.

Development of electrical technology during the last two decades of the nineteenth century, primarily the introduction of the transformer and polyphase circuits, led to the use of alternating current. Numerous advantages of ac systems over dc, for example in long distance high voltage transmission, soon became apparent and led to the decline and, eventually, to near elimination of direct current systems.

As the demand for electric energy steadily increased, so did the need for bulk power transmission over long distances. New technologies, appearing after the middle of this century, in particular the development of solid state power devices, helped revive the interest in direct current application and again made dc power transmission a viable alternative. In this chapter an overview of high voltage direct current (hvdc) transmission systems is presented. The historical development and major application areas of hvdc systems is briefly outlined.

The objective of this research is to address one of the problems associated with the operation of conventional hvdc systems, namely commutation failures in hvdc inverters

connected to weak ac systems. This problem has been subject to considerable scrutiny in the literature in recent years. In the final part of this chapter, some previous solution approaches are reviewed.

Development and Application of Hvdc

The first modern commercial hvdc transmission project was introduced in Sweden in 1954. This system connected the island of Gotland to the Swedish mainland. It used mercury-arc valves in 6-pulse monopolar configuration and was rated for 20 MW at 100 kV. A single-conductor submarine cable spanned the 96 km (60 mi) distance with sea return. In the Soviet Union, where long distances typically separate hydroelectric sites from the main load centers, experimental hvdc systems were built during the middle of the century. A full-scale 474 km (294 mi) bi-polar dc overhead transmission line was built between Volgograd and the Donets Basin in the early 1960s. It began operation in 1965 at full rating of ± 400 kV, 900 A and 720 MW [10].

During the past thirty years the interest in hvdc transmission has increased significantly. The rate of installed hvdc transmission capacity has risen from averaging about 400 MW/year during the 1960s and early 1970s to approximately 2900 MW/year for the first half of the 1980s [5]. Development of the mercury-arc valve was important in reviving interest in dc power application during the 1930s and 1940s. Introduction of highly reliable thyristor converter circuits with microprocessor based valve controls and 12-pulse bipolar operation has largely contributed to the rapid growth in installed hvdc transmission capacity in recent years. As of 1985, at least twelve hvdc projects around the world, totalling about 17,000 MW, were either under construction or in the planning stages [5].

Power production and distribution with direct current was prevalent before the turn of the century. Central power stations were operated in major cities around the world, supplying dc energy for lighting and industry. The introduction of the transformer, three-phase circuits and the induction motor was primarily responsible for the later ascendancy of alternating current systems. As power and voltage levels increased, ac generators completely replaced the use of dc generators for power production. By interfacing between different parts of the power system, the transformer allowed the use of different voltage levels for generation, transmission, distribution and consumption. The simple and rugged induction motor could be operated at much higher speeds than dc motors and required much less maintenance. Speed was also a major factor in the advance of ac generators, as steam turbines replaced slower-speed steam engines as prime movers.

Early efforts in dc power transmission included development of the so-called Thury systems, named for the French engineer Rene Thury [10]. Interestingly, there were certain similarities between these systems and modern hvdc systems. The Thury systems used a number of series-wound dc generators, in some cases as many as 18, connected in series at the sending end of a transmission line to provide sufficiently high transmission voltage. At the receiving end, a comparable number of dc motors, also connected in series, served as prime movers for both dc and ac power generation and distribution.

High maintenance cost due to mechanical wear of dc machine commutators was a major drawback of the Thury systems, and also affected their energy availability. The mercury arc valve and the solid state thyristor allow a direct, non-mechanical conversion of ac power to dc at the sending end of a transmission link and back to ac at the receiving end.

Compared to conventional three-phase transmission with alternating current, hvdc transmission has both advantages and disadvantages. There are certain technical limita-

tions inherent to ac systems, as for example stability problems in long transmission lines. However, in most practical cases the final choice of dc over ac for bulk power transmission is stipulated by economic rather than technical factors. When existing and planned hvdc projects are considered, following scenarios emerge as principal application areas for hvdc transmission:

- Long water crossings involving submarine cables
- Asynchronous or dual-frequency connections
- Bulk power transmission over long distances
- Transmission from remote generation areas
- Stability enhancement of the surrounding ac network

The primary advantages of hvdc compared to conventional ac transmission can be summarized as follows:

- Lower line losses
- More economical overhead transmission lines
- Higher power density for a given transmission right-of-way
- Elimination of long transmission line instability
- Asynchronous tie between ac systems with different operating frequencies
- Direct control of power flow
- Elimination of reactive power compensation of long transmission lines
- Reduction of short-circuit capacity of ac system circuit breakers in interconnected ac/dc systems
- Higher reliability in bipolar operation

Main limitations of hvdc transmission are as follows:

- High cost of converter stations

- Generation of undesirable harmonics both on the ac side and the dc side of the system
- High demand for reactive power compensation at converter stations
- Commutation failure problems in line-commutated inverters connected to weak ac systems
- Difficulty with dc interconnections

Objectives of Research

An integral part of the operation of hvdc converters is the commutation of the dc current between converter valves. The probability of inverter commutation failure is a major concern in the overall design of hvdc systems. Line-commutated inverters are likely to experience commutation failures during transients in the inverter bus voltage. This problem is further aggravated if the inverter is connected to a relatively weak (low short-circuit ratio) ac network [1,7,9,11,13,14,15,16]. Extension of hvdc systems to 3 or more terminals (multiterminal operation) will also lead to more severe consequences of commutation failures, particularly at low rated terminals [11,18,20,21].

The causes of commutation failure in an hvdc inverter are very complex, depending on a number of factors in the system. Three basic causes are (1) a sudden transient reduction in the commutation voltage, (2) a rapid rise in the direct current, both of which can occur due to various disturbances in the ac and dc circuits of the system, and (3) a delayed or missing valve firing pulse, which can result from a malfunction in the converter control circuitry.

A leading cause of commutation failure comes from the occurrence of a severe fault in the ac network, resulting in a transient depression of the inverter bus voltage. The magnitude of the voltage disturbance, the time of occurrence of the fault relative to the

commutation voltage wave, and the transient response of the ac system are all important factors that may contribute to failures.

The severity of the voltage disturbance depends on several factors, including the location and type of fault, local network impedances and the SCR (short-circuit ratio) of the ac commutating bus. The short-circuit ratio is defined as the ratio between the short-circuit capacity of the ac system at the inverter bus and the dc power rating of the inverter. The time of occurrence of the fault is a random event, making failures at times unavoidable since the disturbance may occur at the most sensitive time. For example, if the fault occurs close to a valve gate pulse, control action will not be effective for that valve when the next commutation should occur and a failure may result if the voltage depression is large enough.

The transient response of the ac network during and after a fault is also an important factor in determining the likelihood of commutation failure. As will be shown later in this report, the transient voltage response is made up of two components: (1) the sudden exponential change in the fundamental voltage and (2) the underdamped oscillations which are comprised of the remaining harmonics. The first component is sensitive to the location of the fault and the SCR of the commutating bus. The second component is affected by local network impedances and ac harmonic filters, but is particularly sensitive to the size of capacitor banks located at the inverter bus. It is the second component, related to the frequency spectrum of the ac network and its influence on the commutation process, which is the main topic of this research. As illustrated in the following chapters, the frequency spectrum plays a crucial role in causing commutation failures in hvdc inverters.

It is not unusual for the surrounding ac network at an inverter terminal to have a low frequency dominant mode of oscillation in the 160–220 Hz range. Even lower dominant

frequency modes have been observed in practice [21]. Later in this report it will be shown that by increasing the frequency of the dominant oscillatory response of the ac system, it is possible to increase the net commutation voltage following a fault and thus shorten the required commutation period and reduce the risk of failure.

The goal of this study is minimization of the probability of commutation failure in an HVDC inverter connected to a weak ac system, given specific system operating conditions. To accomplish this the following steps are proposed:

- 1 Determine the sensitivity of commutation failures to variation in system parameters and identify a feasible set of system variables and their constraints for optimization purposes.
- 2 Specify an objective function (cost function) with variables selected in step 1, that measures the likelihood of commutation failure.
- 3 Design a computer algorithm that will minimize the cost function subject to specified variable constraints.
- 4 Perform computer simulations of an integrated ac/dc test system to verify the performance of the optimum solution.

Previous Work

In spite of the significance of commutation failure problems in hvdc systems, there are relatively few alternatives for improving system performance. Larger smoothing reactors at inverters may help alleviate the problem by limiting the rate of rise of direct current. Increasing the SCR at the inverter bus may also help by reducing the magnitude of voltage dips during ac disturbances. The inverter can be operated at larger margin angles in order to allow more time for the commutation process and thus reduce the likelihood of failure, although this may be undesirable in many cases because of increased reactive

power demand at the inverter. Larger shunt capacitors could be installed at the inverter bus to meet the increased VAR demand, but this obviously increases the cost of the installation. It also lowers the short circuit ratio and the dominant frequency mode of the ac system and increases the risk of commutation failure.

Various types of converter controls have been cited in the literature that quickly advance the valve gating angle when disturbances are sensed in order to prevent commutation failure. J. Arrillaga et al. [3] propose to use direct digital control for optimum performance of static converters, with considerable advantages over analog-based methods in terms of speed, accuracy and reliability. Firing pulses are generated on the bases of numerical processing of system state measurements. Among cited advantages are extreme accuracy in valve firing (down to 1/10th of a degree), direct frequency and phase locking to the commutating voltages for maintaining synchronism, good accuracy in extinction angle and direct current measurements and general flexibility and veratility of the control system.

R. J. Piwko et al., in a more recent study [15], describe control techniques designed especially to allow stable operation of hvdc converters connected to ac systems with low short-circuit ratio or weak ac systems. Ac voltage and power instability is an inherent problem associated with such interconnections, which enhances the likelihood of commutation failure. The new microprocessor-based control scheme can be used both for rectifiers or inverters and has been implemented in two different hvdc installations. Some outstanding features of the system are (1) an ac voltage regulator that operates through the direct voltage and current regulators, (2) reactive compensation controllers that switch compensation elements to regulate the converter control angles within desired limits, (3) converter transformer tap changer controls that regulate direct voltage and/or

current to within a desired range and (4) an ac voltage flicker control to reduce the abrupt changes in ac bus voltage caused by the switching of reactive compensation elements.

Linearized system models or state-space techniques have been used to design optimal or sub-optimal inverter controllers utilizing feedback of system parameters, such as bus voltage and direct current, or using tracking and eigenvalue search techniques for determining controller feedback gains and other controller parameters for best performance. M. S. Sachdev et al. [19] apply modern control theory for optimal hvdc controller design. Eigenvalues of the linearized system are calculated and tracked as system parameters vary. The desired system performance is described by a cost function which is minimized by a state regulator for optimal results.

D. P. Carroll et al. [6] use eigenvalue analysis to compare the performance of combined dc voltage and dc current feedback for converter control with the use of a conventional dc current regulator. The alternate control scheme contains the same basic features used in the conventional controller, but includes a voltage feedback loop using local measurements of the dc voltage. Results of this study indicate that the voltage feedback offers greater damping of system oscillations and significantly faster large-signal response than the conventional regulator.

Adaptive control is proposed by S. Lefebvre et al. [12] as an alternative to converter controllers with fixed gain. The controller, which is tuned to variations in system topology, is supposed to improve the dc system dynamic response. Various forms of commutation margin controls are also described which generally involve an estimate and feedback of the commutation margin angle [4,8]. The use of VDCL (voltage dependent current limit) characteristics in the converter controls have also been effective during fault recovery [2,4,16,17,18,20,21].

J. Reeve and S. P. Chen introduce a new approach to digitally model the transient response of ac/dc power systems to disturbances [17]. The digital simulator is based on EMTP (Electro-Magnetic Transients Program) on a mainframe computer operating in parallel with a microcomputer containing a detailed converter control model with user-interactive capabilities. The paper emphasizes the need for detailed and accurate modeling of the integrated ac/dc system. In a follow-up paper [18] the same authors demonstrate the use of the digital simulator on a 4-terminal hvdc system with one inverter connected to a weak ac system. Different types of faults are inflicted on the system and the system recovery times are examined. The simulation results indicate that commutation failures assume an increased significance in parallel multiterminal system environment, and that the use of LVDCOL (low-voltage-dependent-current-order-limit) at each rectifier proves beneficial to system recovery. Another simulation study is reported by R. Adapa and J. Reeve [1] in which the complex interaction between a dc transmission system and a weak ac system is investigated during various types of ac system faults. Patterns of valve conduction are identified and traced in detail through a fault period and up to system recovery to provide insight into the precise interaction during a disturbance.

A simulation study of a proposed multiterminal hvdc system stretching between the La Grande 2 complex in Quebec and Sandy Point in Massachusetts is reported by V. K. Sood et al. [21]. The study focuses on the impact of harmonics on the transient performance of the system and on the control and protection strategies. In particular, it establishes a strong sensitivity of one inverter station to the second harmonic resonance on the ac side and 60 Hz resonance on the dc side. Simulations indicate that this particular inverter is prone to commutation failure. The use of larger smoothing reactors shows some benefits in limiting the injection of 60 Hz and dc harmonics into the dc line at the inverter, although by itself it is not considered adequate to eliminate the probability of commutation failure. The use of a second harmonic filter is rated detrimental to the

recovery following a disturbance, whereas dc controls based techniques were successfully utilized during the recovery period.

Regardless of the technique used, there is usually some combination of events under which feedback controllers alone cannot prevent commutation failure. To bypass some of the problems of operating hvdc systems into weak ac networks, K. Tam and R. Lasseter [22] propose the use of a hybrid inverter. In this type of inverters the commutation process is not as sensitive to transients in the inverter bus voltage as in a line-commutated inverter. Auxiliary circuits, often in the form of charged capacitors, are used to extend the available commutation interval.

CHAPTER 2

HVDC SYSTEM MODELING AND ANALYSIS*

Introduction

The primary role of hvdc converter stations is to convert ac power over to dc at the sending end of a transmission link (rectification) and back to ac at the receiving end (inversion). This conversion back and forth is accomplished by the use of high power switching circuitry. Mercury arc valves were used exclusively as switching elements in the first commercial hvdc converters. In all modern installations however, the mercury arc valves have been replaced by solid state thyristors.

The switching of the ac current between converter valves to accomplish unidirectional current flow for dc operation is called commutation. Both mercury arc valves and thyristors operate with basically the same logic. A negative grid voltage or zero gate current holds off the device and a positive control pulse turns it on if the anode-to-cathode voltage is positive. Turn-off however, can be effected only by a natural zero crossing of the current in the converter circuit.

Converter control is intrinsic to the operation of an hvdc transmission system. Not only is the control of the converter valves required for the regulation of normal transmission, but it is also useful for system protection. The controls for hvdc systems are usually organized in a hierarchical structure. On the base level of the control hierarchy is the generation of voltage or current pulses for ignition of the mercury arc valves or gating of the thyristor valves.

* Based in part on EEL 5934 Spring 1986 class notes, Ch. 2, by D.P.Carroll

If a control firing pulse for a particular valve-pair is delayed or missing or if a sudden disturbance occurs in the ac system connected to the hvdc terminal, a commutation failure may result. Commutation failures are quite common, especially in line-commutated inverters, but undesirable since they are a major threat to normal system operation. Commutation failures normally lead to a transient voltage collapse in the affected terminal and a temporary power shut-down on the dc link. The likelihood of a commutation failure during a systems fault depends on several factors in the ac network that connects to the hvdc terminal, as well as factors in the hvdc converter itself. The transient response of the converter bus voltage and the dc current during the fault are two major factors affecting the commutation process. The steady-state operating condition of the hvdc converter immediately prior to a fault, and the performance of the converter controls also play an important role.

In this chapter the theory of hvdc converter operation is presented. Specifically, we will study the characteristics of the two terminal system, comprised of a rectifier at the sending end of an hvdc transmission line and an inverter at the receiving end. The steady state operation of the system is analyzed, and the commutation process and the causes of commutation failure are studied in detail. Finally, we will consider possible ways to reduce the likelihood of commutation failure.

Basic Converter Configurations

Power switching circuits utilizing high power thyristors (SCRs) are extensively used in many industrial applications requiring power conditioning to interface with the electric utility system. Two basic operating principles are used in these circuits, namely, self-commutation and line-commutation. In self-commutated circuits the voltage necessary for commutation, i.e., to route the current from one thyristor valve to the next, is generated

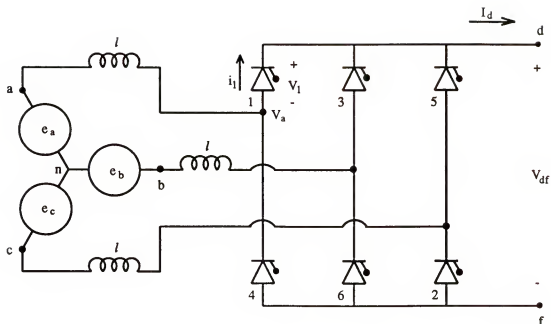


Fig. 2.1 Graetz bridge; conduction sequence 1-2-3-4-5-6.

within the circuit itself, whereas in line-commutated circuits the commutation voltage is derived from the line voltages of the ac network.

Line-commutated converters have been used exclusively in all existing hvdc transmission systems, to interface with the ac utility network. This is mainly due to the higher losses associated with many self-commutated converters and, to some extent, the proven reliability of the less complex line-commutated circuits.

The basic building block for nearly all existing and planned hvdc converters is the three-phase Graetz bridge shown in Fig. 2.1, which illustrates a typical six-pulse converter. Compared to other line-commutated circuits, the Graetz bridge provides the

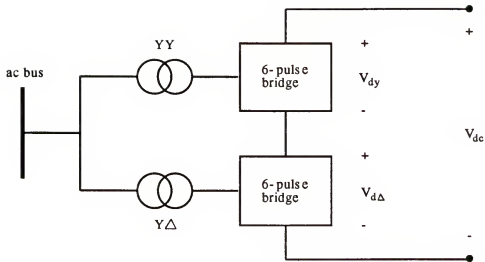


Fig. 2.2 Twelve pulse converter.

best overall transformer utilization. Most newer hvdc systems use twelve-pulse circuits, which are a combination of two six-pulse Graetz bridges connected in series through wye-wye and wye-delta transformers as shown in Fig. 2.2. The twelve-pulse approach offers a substantial gain over six-pulse converters, both economically and technically. Twelve-pulse operation offers twice as high transmission voltage and thus lower losses, and the 30° phase shift between the transformer banks eliminates some of the lower order harmonics. The following analysis relates to the six-pulse bridge but will subsequently be extended to twelve-pulse converters.

Steady-State Analysis

Since the six-pulse bridge is composed of switching components, i.e. the thyristor valves, the circuit topology is continually changing and a general time function analysis is extremely difficult. The valves are normally gated in an equal-interval switching sequence with gating pulses separated by 60° or $1/6$ cycle. Since this switching rate is much higher than the ac system frequency, an average value analysis is sufficient and useful for many applications. The major effect lost when this form of converter modeling is used, is the effect of characteristic harmonics generated by the circuit. In the subsequent analysis the following assumptions are made:

- The commutation angle is limited to 60° or less.
- The direct current is constant.
- The ac supply voltages are sinusoidal.
- Valves are ideal switches.
- Transformer magnetizing currents are neglected.

The first assumption means that the commutation process will be completed within the 60° spacing of the gating pulses, as illustrated in Fig. 2.3, and thus, only one commutation will occur at a time. This also implies that no more than three valves can conduct simultaneously in normal operation. The assumption of constant direct current and purely sinusoidal ac voltages are very nearly true in a real hvdc system as a result of tuned harmonic filters used on both the ac and dc sides of the system.

Before analyzing the Graetz bridge shown in Fig. 2.1, it is helpful to review the magnitude and phase relationships of the ac supply voltages. These relationships are summarized in Fig. 2.4 which shows a phasor diagram of the three line-neutral voltages e_a , e_b and e_c , with a phase separation of 120° . Also shown are the six line-line voltages

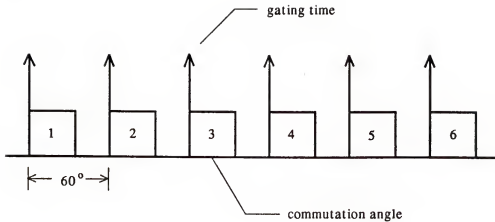


Fig. 2.3 Commutation angles during mode 1 operation.

e_{ab} , e_{ac} , e_{bc} , e_{ba} , e_{ca} and e_{cb} , which are separated in phase by 60° . As will be illustrated in the following analysis, these line-line voltages are sequentially connected to the dc terminals by the switching of the converter valves.

First consider the idealized case where the gating voltage of all valves is permanently “on”, and the bridge operates as if it consisted of diodes. Also, let us initially neglect the effects of the per phase transformer leakage reactance. Under these assumptions, upper bridge valves 1, 3 and 5 successively conduct the constant direct current as the positive-half phase voltages e_a , e_b and e_c cross each other and forward-bias the valves. Likewise, lower bridge valves 4, 6 and 2 successively conduct as the negative-half phase voltages

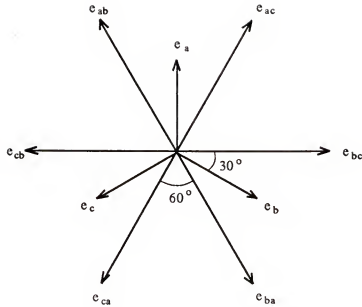


Fig. 2.4 Relationship between line-neutral and line-line supply voltages.

cross. Fig. 2.5 shows a sketch of the bridge voltages and currents for this idealized case. The variables shown are identified in Fig. 2.1. The sketches in the upper portion of Fig. 2.5 are superimposed on a time plot of the line-neutral and line-line voltages shown in Fig. 2.4. Since the bridge circuit is a full-wave converter, the line-line voltages shown in Fig. 2.5 appear as a “six-phase” set. Note also that the timing marks on the lower part of Fig. 2.5 are reference points spaced 60° apart, which corresponds to each crossing of the supply voltages. The voltages V_{dn} and V_{fn} are measured from points d and f on the dc side of the bridge to the ac neutral point n. The direct voltage across the bridge, V_{df} , is simply the difference $V_{dn} - V_{fn}$. In this idealized case where the valves behave like diodes, V_{dn} rides along the top of the line-neutral waves as valves 1, 3 and 5 become forward-biased, and V_{fn} rides along the bottom of the voltage waves as valves 4, 6 and 2 become forward-biased. The voltage V_l is the voltage across valve 1, which is zero when

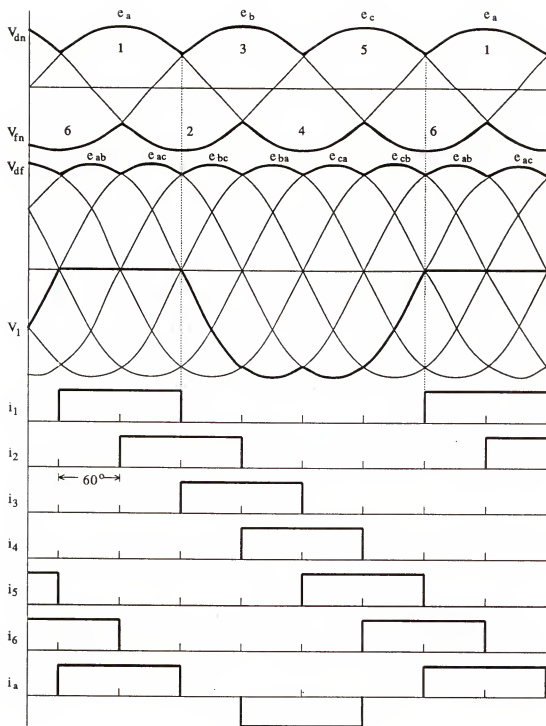


Fig. 2.5 Voltage waveforms for idealized bridge operation.

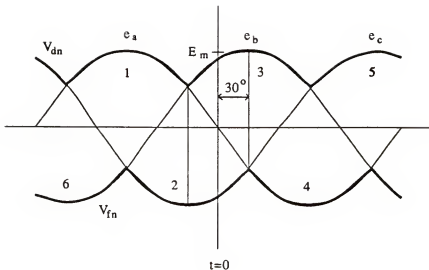


Fig. 2.6 Voltage waveforms for calculation of bridge output voltage.

valve 1 is on and is equal to $e_a - V_{dn}$ when valve 1 is off. V_{dn} is equal to e_b when valve 3 is on and e_c when valve 5 is on. The peak inverse voltage across valve 1 is therefore determined by line-line voltages e_{ab} and e_{ac} . In this idealized case the valve currents are rectangular pulses, as the direct current is instantaneously switched between phases. In reality, the current takes a finite time to transfer between valves due to the inductance in each phase, which gives rise to the commutation angle. As further analysis will show, the commutation process has a rounding effect on the waveshapes of valve currents.

The average of the bridge output voltage V_{df} can be found for the idealized case by integrating over 60° of the supply voltage waveform, as indicated in Fig. 2.6. The phasor diagram of the corresponding voltages is shown in Fig. 2.7. For the assumed time interval shown in Fig. 2.6, the bridge output voltage is given by

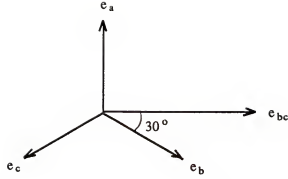


Fig. 2.7 Voltage relations for ideal operation.

$$V_{df} = e_{bc} = \sqrt{3}E_m \cos \omega t, \quad -\frac{\pi}{6} \leq \omega t \leq \frac{\pi}{6} \quad (2.1)$$

The average voltage for the idealized case is therefore

$$V_{d0} = V_{df}^{avg} = \frac{3}{\pi} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \sqrt{3}E_m \cos(\omega t) d(\omega t) = \frac{3\sqrt{3}}{\pi} E_m \quad (2.2)$$

In reality the output of the bridge voltage is controlled by delaying the gating of each valve by an angle α . This is accomplished by varying the time at which each gating voltage pulse turns on, after the respective phase voltage crossings forward-bias

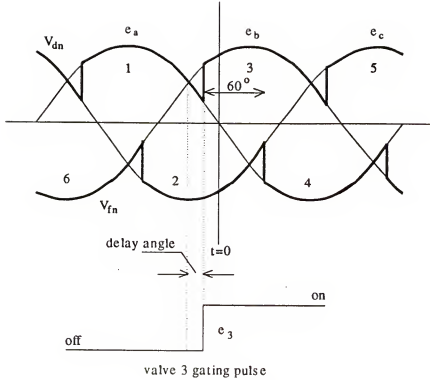


Fig. 2.8 Effect of gating delay angle on voltage waveforms.

the valves. This is illustrated in Fig. 2.8, where the gating pulse for valve 3 is shown along with the modified waveforms for V_{dn} and V_{fn} . In this case the average value of V_{df} is again computed by integrating over 60° , but the interval must be changed to account for the delay angle α .

$$V_{df} = \sqrt{3}E_m \cos \omega t, \quad -\frac{\pi}{6} + \alpha \leq \omega t \leq \frac{\pi}{6} + \alpha \quad (2.3)$$

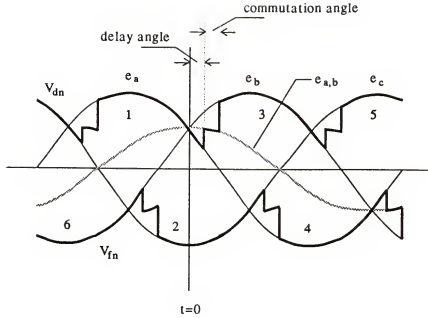


Fig. 2.9 Voltage waveforms with delay angle and commutation angle.

$$V_d = V_{df}^{avg} = \frac{3}{\pi} \int_{-\frac{\pi}{6} + \alpha}^{\frac{\pi}{6} + \alpha} \sqrt{3} E_m \cos(\omega t) d(\omega t) = \frac{3\sqrt{3}}{\pi} E_m \cos \alpha \quad (2.4)$$

Equation (2.4) shows that the average direct voltage of the bridge can be varied from its maximum of V_{d0} to some lower value determined by the delay angle α .

Now consider the series reactance of the transformer which feeds the converter bridge. With the assumption of purely sinusoidal supply voltages, the commuting reactance is equivalent to the transformer reactance. However, in general, the total commuting reactance will also include the equivalent ac system impedance. With regard to bridge operation, the commuting reactance has the effect of delaying the transfer of current from one valve to the next, since the current in an inductance cannot

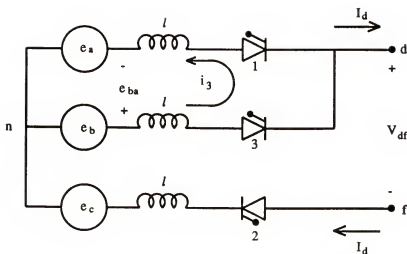


Fig. 2.10 Equivalent circuit for commutation from valve 1 to valve 3.

be changed instantaneously. This delay process results in the commutation angle μ , also called the overlap angle. Fig. 2.9 shows how the commutating reactance affects the bridge voltage waveforms. The analysis of this effect is facilitated by use of the equivalent circuit of the bridge during normal commutation, which is shown in Fig. 2.10 for commutation from valve 1 to valve 3. Fig. 2.11 shows the phasor relationship of the pertinent voltages. The line-line voltage e_{ba} drives the commutating current i_3 and is thus called the commutating voltage.

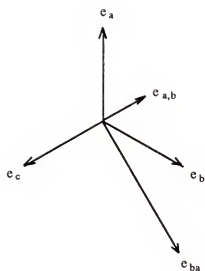


Fig. 2.11 Pertinent voltages during commutation from valve 1 to valve 3.

From the equivalent circuit in Fig. 2.10 the commutation current i_3 can be derived as

$$2l \frac{di_3}{dt} = e_{ba} \quad (2.5)$$

Assuming a commutation voltage of the form

$$e_{ba} = \sqrt{3}E_m \sin \omega t, \quad \alpha \leq \omega t \leq \alpha + u \quad (2.6)$$

equation (2.5) may be integrated to give

$$i_3(t) = \frac{1}{2l} \int_{\frac{\alpha}{\omega}}^t e_{ba}(\tau) d\tau = \frac{\sqrt{3}E_m}{2l} \int_{\frac{\alpha}{\omega}}^t \sin \omega \tau d\tau + i_3\left(\frac{\alpha}{\omega}\right) \quad (2.7)$$

Since commutation to valve 3 begins at $t = \alpha/\omega$ the current i_3 is still zero at that point, and the right hand term in equation (2.7) thus vanishes, leaving the expression

$$i_3(t) = \frac{\sqrt{3}E_m}{2\omega l} (\cos \alpha - \cos \omega t), \quad \alpha \leq \omega t \leq \alpha + u \quad (2.8)$$

At $\omega t = \alpha + u$, commutation is completed and $i_3 = I_d$, therefore (2.8) gives an expression for the direct current I_d

$$I_d = \frac{\sqrt{3}E_m}{2\omega l} [\cos \alpha - \cos(\alpha + u)] \quad (2.9)$$

During commutation, the voltage drop across the commutation impedance can be expressed as

$$\Delta V_{df} = l \frac{di_3}{dt} = \frac{e_{ba}}{2} = \frac{\sqrt{3}}{2} E_m \sin \omega t, \quad \alpha \leq \omega t \leq \alpha + u \quad (2.10)$$

The upper half bridge voltage is therefore

$$V_{dn} = e_b - \Delta V_{df} = e_{a,b} = \frac{e_a + e_b}{2} = -\frac{e_c}{2} = \frac{E_m}{2} \cos \omega t, \quad \alpha \leq \omega t \leq \alpha + u \quad (2.11)$$

which is indicated by the dashed line in Fig. 2.9. Also during commutation, the bridge terminal voltage V_{df} is given by

$$V_{df} = V_{dn} - V_{fn} = -\frac{3}{2}e_c = \frac{3}{2}E_m \cos \omega t, \quad \alpha \leq \omega t \leq \alpha + u \quad (2.12)$$

The bridge terminal voltage may also be written

$$V_{df} = \begin{cases} e_{bc} - \Delta V_{df}, & \alpha \leq \omega t \leq \alpha + u \\ e_{bc}, & \text{remainder of interval} \end{cases} \quad (2.13)$$

Therefore, the average bridge voltage may be obtained by averaging the effect of ΔV_{df} and subtract the result from equation (2.4). This gives the expression

$$V_d = V_{d0} \cos \alpha - \frac{3}{\pi} \int_{\alpha}^{\alpha+u} \frac{\sqrt{3}}{2} E_m \sin(\omega t) d(\omega t) \quad (2.14)$$

which reduces to

$$V_d = V_{d0} \cos \alpha - \frac{3\sqrt{3}E_m}{2\pi} [\cos \alpha - \cos(\alpha + u)] \quad (2.15)$$

This can also be written

$$V_d = \frac{V_{d0}}{2} [\cos \alpha + \cos(\alpha + u)] \quad (2.16)$$

Equation (2.16) may be combined with (2.9) to form an alternate voltage equation

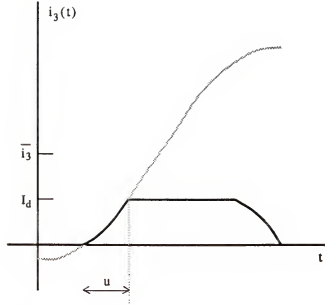


Fig. 2.12 Valve current waveshape during commutation.

$$V_d = V_{d0} \cos \alpha - \frac{3\omega l}{\pi} I_d = \frac{3}{\pi} \left[\sqrt{3} E_m \cos \alpha - X_l I_d \right] \quad (2.17)$$

where X_l denotes the commutation reactance.

In addition to modifying the bridge voltage, the commutation process also affects the waveshape of the individual valve currents. For example, Fig. 2.12 shows one possible waveshape for valve 3 current as obtained with the help of equation (2.8). The dashed line indicates the many possible curvatures that may result for different delay angles.

Rectifier and Inverter Operation

The gating delay angle α may theoretically range from 0° to 180° , since the commutation voltage across each valve remains positive for that period. However, to allow for a reasonable commutation angle, α must be restricted to somewhat less than 180° in practice. Rectifier operation is defined by a positive ac to dc power flow, and thus a positive terminal voltage. Inverter operation is just the opposite, and is defined by negative ac to dc power flow, and hence requires a negative bridge terminal voltage. The transition angle α_t , which separates rectifier and inverter operation, is defined as that delay angle which produces $V_d = 0$, and thus from equation (2.16)

$$\cos \alpha_t = -\cos(\alpha_t + u) = \cos[\pi - (\alpha_t + u)] \quad (2.18)$$

or

$$\alpha_t = \pi - \alpha_t - u = \frac{\pi - u}{2} \quad (2.19)$$

Generally rectifiers are operated with small delay angles for economic reasons, so typically $\alpha < 15^\circ$. Fig. 2.13 illustrates the bridge voltage and current waveforms for rectifier operation, as defined in the circuit diagram of Fig. 2.1.

As stated above, inverter operation differs from rectification only in the size of the gating delay angle α . Inversion is associated with a negative bridge terminal voltage V_d which corresponds to a large delay angle. The voltage waveforms for inversion are illustrated in Fig. 2.14. The extinction advance angle γ is defined by

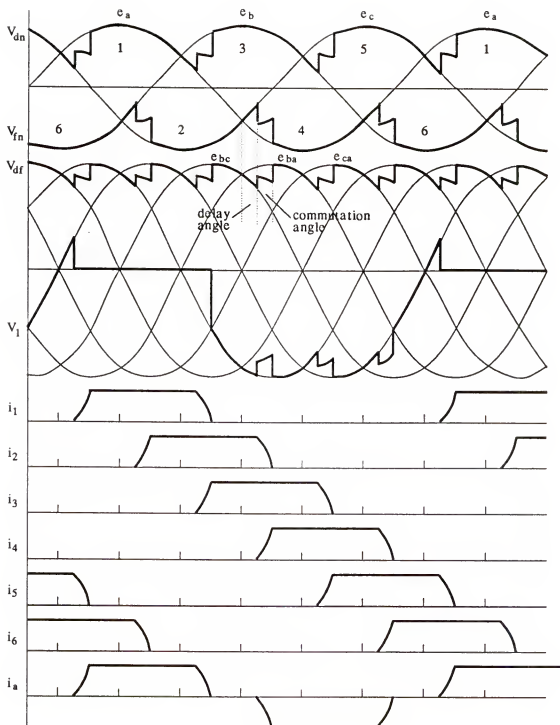


Fig. 2.13 Voltage waveforms for rectification.

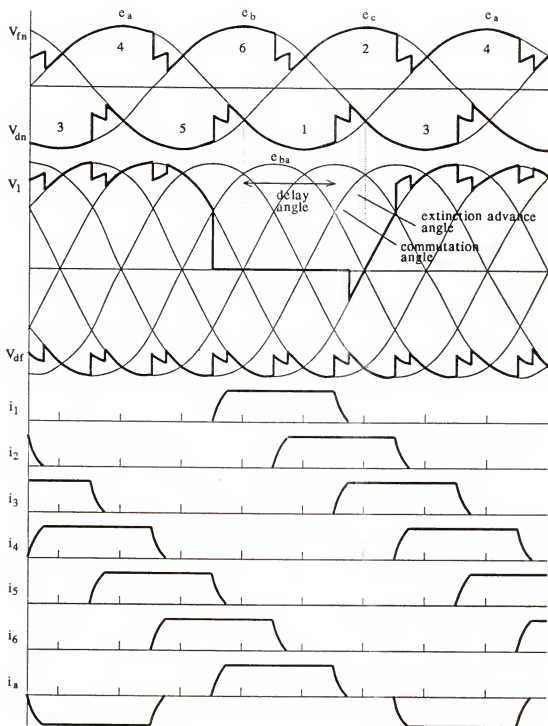


Fig. 2.14 Voltage waveforms for inversion.

$$\gamma = \pi - (\alpha + u) \quad (2.20)$$

where α and u are the delay angle and the commutation angle respectively.

An important difference between rectification and inversion is apparent from Figs. 2.13 and 2.14. Since the angle γ is much smaller for inverter operation, the period of inverse voltage across a valve is correspondingly smaller. Therefore, the time available for valve turn-off (the commutation margin) may be quite limited during inversion. If the commutation margin angle is not sufficient for turn-off of the outgoing valve, a commutation failure will result. This phenomena is analysed in detail later in this chapter.

Equivalent Circuits and Control of Two-Terminal System

For the purposes of illustrating the operation of a basic dc link, assume that each of the two converter terminals consist of a single 6-pulse bridge. The average value analysis presented in the previous sections provides simple and convenient equivalents for the analysis of the two-terminal system. Equation (2.17) represents the average terminal voltage of the rectifier and can be interpreted as a voltage-behind-resistance model. The no-load voltage is given by

$$V_{nl(rec)} = \frac{3\sqrt{3}}{\pi} E_m \cos \alpha \quad (2.21)$$

and the equivalent “resistance” is

$$R_{cr} = \frac{3X_{lr}}{\pi} \quad (2.22)$$

where X_{lr} is the equivalent commutation reactance of the rectifier. Note that equation (2.22) seems to be dimensionally incorrect. R_{cr} , however, is actually a reactance as the equation indicates and not a true resistance. When equation (2.17) is interpreted as a linear dc model, R_{cr} appears as a “dc” impedance.

To obtain a similar model for the inverter, we can use equation (2.16) along with equation (2.20) to get

$$V_d = -\frac{V_{d0}}{2} [\cos \gamma + \cos (\gamma + u)] \quad (2.23)$$

Similarly, by combining equations (2.9) and (2.20) we get for the direct current

$$I_d = \frac{\sqrt{3}E_m}{2\omega l} [\cos \gamma - \cos (\gamma + u)] \quad (2.24)$$

Finally, by solving equations (2.23) and (2.24) together and using equation (2.2) for V_{d0} , we get the average terminal voltage for the inverter as

$$V_d = -V_{d0} \cos \gamma + \frac{3X_{li}I_d}{\pi} \quad (2.25)$$

In this case the no-load voltage is

$$V_{nl(inv)} = -\frac{3\sqrt{3}}{\pi} E_m \cos \gamma \quad (2.26)$$

and the equivalent “resistance” is

$$R_{ci} = -\frac{3X_{li}}{\pi} \quad (2.27)$$

The combined equivalent diagram for both terminals and the transmission line is shown in Fig. 2.15. Note that the inverter must be connected “up-side-down” in order to comply with the unidirectional current flow through the system. Also note that there are no real power losses in the equivalent “resistances” R_{cr} and R_{ci} . As pointed out earlier, these are fictitious resistors used for convenience to model the equivalent “drop” in the average converter voltage as expressed in equations (2.17) and (2.25). This is illustrated by the graphs in the lower part of Fig. 2.15. The difference between $V_{d(rec)}$ and $-V_{d(inv)}$ is the voltage drop due to R_l , the resistance of the transmission line.

In order to enable overall control of the dc link in a realistic setting, each terminal is provided with a feedback regulator. Fig. 2.16 illustrates the combined control characteristics for both converters. In normal operation the rectifier supplies power to the dc line under constant current (CC) control, while the inverter receives power from the dc line under constant extinction angle (CEA) or constant gamma control. In this way the inverter determines the system voltage, while the rectifier determines the current. The actual operating point is determined by the intersection of the two control characteristics, in this case at point A. The regulators at each terminal can switch roles; for example, if the ac voltage at the rectifier bus drops to a lower level, as indicated by the dotted line in Fig. 2.16. Under these conditions the inverter would determine the current in constant current control, while the rectifier would determine the system voltage in constant ignition angle (CIA) or constant beta control. The ignition advance angle β is defined as

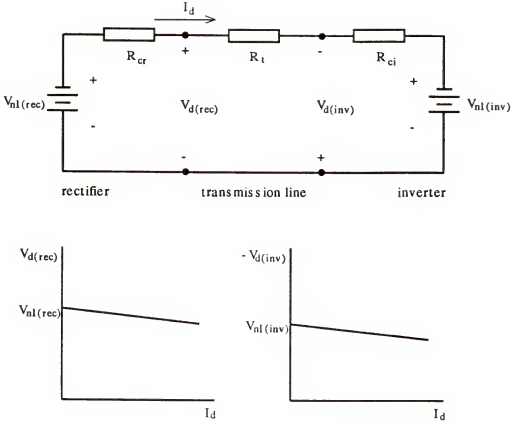


Fig. 2.15 Equivalent circuit for two terminal system.

$$\beta = \pi - \alpha \quad (2.28)$$

The new operating point in this case would be located at B. The difference in the dc current between operating points A and B is called the current margin and is typically adjusted to 15% of the nominal system current. This is to allow each terminal to operate in constant current control without interference from the other terminal. The transfer of operation from point A to point B is called mode shift.

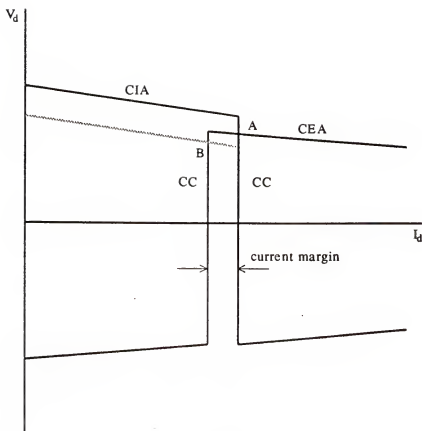


Fig. 2.16 Control characteristics for two terminal system.

In the simple dc link being analysed here, the two converters are assumed to be compatible. Power can be transmitted in either direction depending on the operating condition at each terminal. Rectification or inversion is dictated solely by the gating delay angle α , as indicated in the previous section. In Fig. 2.15 the direction of power flow is from the rectifier to the inverter. This is achieved by virtue of an operating point with a positive voltage polarity as shown in Fig. 2.16. Power reversal can be accomplished simply by moving the operating point over to the negative voltage region.

This is implemented by transferring the current margin from the inverter over to the rectifier. As a consequence, the terminal voltages of both converters decrease rapidly and become negative as a new operating point is established.

Twelve-Pulse Converters

In the previous sections we have focused our attention on the six-pulse converter. Most newer hvdc installations, however, use twelve-pulse converter units. As shown in Fig. 2.2, the twelve-pulse converter consists of two six-pulse Graetz bridges connected in series through wye-wye and wye-delta transformers. The average value analysis performed in the previous sections can therefore easily be modified to apply to the twelve-pulse converter.

Referring to Fig. 2.2, the overall direct voltage V_{dc} is doubled, with a reduced dc ripple due to the 30° phase shift between the two six-pulse voltage outputs V_{dy} and $V_{d\Delta}$. The average terminal voltage is therefore given by

$$V_d = \frac{6\sqrt{3}}{\pi} E_m \cos \alpha - \frac{6X_l}{\pi} I_d \quad (2.29)$$

Due to the series connection of the two six-pulse bridges, the direct current I_d is common to both circuits. Also, assuming that both bridges share the same gating delay angle α and that the transformer reactances are identical, the expression relating I_d with the converter angles does not change for twelve-pulse operation. Consequently, I_d is still given by equation (2.9).

Commutation Failures

The focus of this study centers around the commutation process in line-commutated inverters. Commutation failures are common in practice and are of major concern in hvdc system operation. The problem is further aggravated if the inverter is connected to a weak ac system due to excessive voltage excursions on the inverter bus during a system fault. In this section we will analyse the basic mechanism of the commutation process in more detail.

Consider again the simplified equivalent circuit shown in Fig. 2.10, which portrays commutation in a line-commutated inverter, in this case from valve 1 to valve 3. The voltages are the fundamental components of the supply voltages at the ac bus, and the inductances represent the idealized short-circuit reactances at the bus. The commutation current i_3 is given by

$$i_3(t) = \frac{1}{2l} \int_{t_3}^t e_{ba}(\tau) d\tau \quad (2.30)$$

where t_3 denotes the beginning of commutation (gate time of valve 3), and it is assumed that $i_3(t_3) = 0$. When commutation is complete, i_3 will have reached the value of the direct current I_d , which defines the commutation angle u . Therefore, we get the expression

$$I_d = \frac{1}{2X_l} \int_{\alpha}^{\alpha+u} e_{ba}(\omega t) d(\omega t) \quad (2.31)$$

where X_l is the commutation reactance and α is the gating delay angle. For commutation to be successful, equation (2.31) shows that a minimum amount of volt-degrees are needed. For example, if the voltage e_{ba} decreases just before or during commutation,

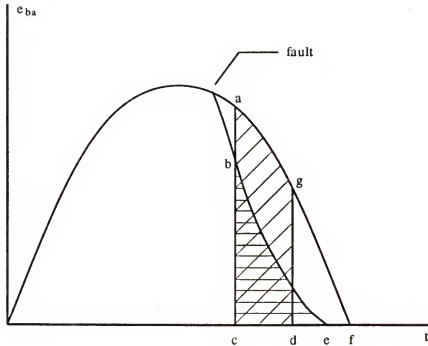


Fig. 2.17 Effect of voltage dip on commutation.

the angle u has to increase in order to satisfy equation (2.31), assuming that the direct current remains constant. However, the commutation interval can only be extended to the point where e_{ba} crosses over to become negative. This is illustrated in Fig. 2.17, where commutation is assumed to start at point c . For the sinusoidal voltage waveform, the shaded area $abcdga$ indicates the volt-degrees needed for commutation, and $gdefg$ is the remaining margin area. If the voltage wave is non-sinusoidal due to a sudden transient, as shown also in Fig. 2.17, the commutation and margin areas can be adversely effected. In this case, if the shaded area $bcdeb$ is less than $abcdga$, commutation failure will occur.

Among the tasks assigned to the converter control system is the generation of valve firing pulses to start each commutation. In a line-commutated inverter, the gating pulses

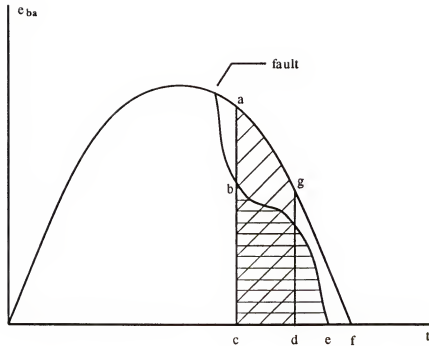


Fig. 2.18 Effect of voltage oscillation on commutation.

are synchronized to the ac system frequency, and are thus generated at equally spaced intervals in steady-state operation. In a case of disturbance, for example, if the inverter bus voltage suddenly drops or the direct current increases, the control system will eventually advance the valve gating pulses to compensate for the disturbance. However, if the fault occurs just before commutation is scheduled to begin as indicated in Fig. 2.17, the short lead-time will not allow the control system to react in time for that particular commutation. In that situation, and if the disturbance is severe enough, even a fast-acting predictive type control will not be able to prevent commutation failure.

Equation (2.31) can also be written in the form

$$I_d = \frac{u}{2X_l} \overline{e_{ba}} \quad (2.32)$$

where

$$\overline{e_{ba}} = \frac{1}{u} \int_{\alpha}^{\alpha+u} e_{ba}(\omega t) d(\omega t) \quad (2.33)$$

is the average value of e_{ba} over the commutation period u . The required average commutation voltage is therefore

$$\overline{e_{ba}} = \frac{2X_l I_d}{u} \quad (2.34)$$

Commutation will succeed regardless of the waveshape, as long as the average commutation voltage is large enough over the commutation period. This is illustrated in Fig. 2.18. Compared to Fig. 2.17, where the transient fault voltage consists of a low frequency component, the transient wave in Fig. 2.18 consists of somewhat higher frequency oscillations. This has the effect of increasing the commutation area $bcdeb$ over that of the transient wave in Fig. 2.17. The type of waveform in Fig. 2.18 illustrates the possible benefit of increasing the frequency of the transient oscillation during commutation, if the ac network has naturally low resonant frequency.

CHAPTER 3

EFFECTS OF FREQUENCY SPECTRUM VARIATION AND FILTER OPTIMIZATION

Introduction

It is not unusual for the surrounding ac system at an inverter terminal to have a low frequency dominant mode of oscillation in the 160–220 Hz range. Even lower frequency modes have been observed in practice [21]. This study will concentrate on transient voltage problems as related to the frequency spectrum of the ac network. The goal is to minimize the likelihood of commutation failure in the hvdc inverter for certain types of faults, given specific operating conditions within the ac system. Later in this chapter it is shown that by increasing the frequency of the dominant oscillatory mode of the ac system, it is possible to increase the average commutation voltage during a fault and thus to reduce the commutation period and the risk of failure. The question is what network parameters can be changed, or what elements must be added to the network, in order to accomplish this. A likely candidate seems to be the capacitor bank since the dominant frequency is sensitive to this parameter. However, the size of the capacitor bank is usually dictated by voltage and VAr requirements at the inverter bus. A possible solution is to replace the capacitor with another circuit, which provides the required VAr compensation but shifts the dominant mode of the spectrum to a higher frequency. This chapter describes a method to modify the frequency spectrum of the ac network by substituting for the capacitor bank at the inverter bus a single tuned filter at a low frequency (120–160 Hz). This is shown to reduce the likelihood of commutation failure significantly.

Model for Ac Network at Inverter Terminal

Fig. 3.1 shows a simplified local ac network model typically associated with an hvdc inverter terminal. The model includes local generation, represented by voltage source behind an equivalent ac system impedance (L_{a1} , L_{a2} and R_a) and local loads, modeled as a constant impedance (R_l and L_l), all connected at the inverter bus (bus 1). Remote loads, also modeled as constant impedance loads (R_r and L_r) are connected at bus 2 and supplied from the inverter bus through a 230 kV ac line (R_f and L_f). Also included are 11-th and 13-th harmonic single tuned filters, a broad-band high-pass filter and a capacitor bank for reactive power compensation, as shown in detail in Fig. 3.2. Most of the VAR demand is due to the inverter, particularly when operated at a large margin angle, but some compensation is also needed because of lagging power factor of the local loads. Although most of the required VARs are supplied by the capacitor bank, a portion is also delivered by the harmonic filters, which are capacitive at 60 Hz. At bus 2, a provision is included to produce ac system faults at varying distances from the inverter bus, including single-phase, three-phase and line-to-line faults. The twelve-pulse hvdc inverter is connected to bus 1 through Y-Y and Y- Δ converter transformers. The nominal circuit parameters used in the studies involving this network are given in Table 3.1.

The short-circuit capacity of the inverter bus can be expressed in simplified form as

$$SCC = \frac{|V_1|^2}{|Z_a|} \quad (3.1)$$

where Z_a is the ac system equivalent impedance given by

$$Z_a = j\omega L_{a2} + (R_a / j\omega L_{a1}) \quad (3.2)$$

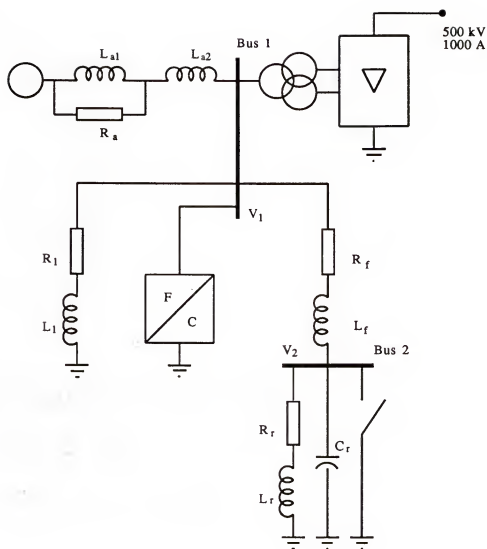


Fig. 3.1 Inverter terminal in test system model.

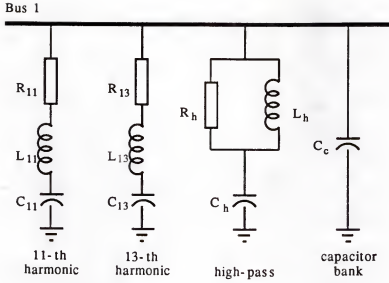


Fig. 3.2 Harmonic filters and capacitor bank at inverter bus.

This is justified, since the ac line and the local load impedances are big compared to Z_a . The short-circuit ratio (SCR) of the ac/dc system interconnection is defined as

$$SCR = \frac{SCC}{P_{dc}} = \frac{\frac{|V_1|^2}{Z_a}}{V_{dc}I_{dc}} \quad (3.3)$$

where P_{dc} is the rated power of the inverter terminal. The harmonic filters and the capacitor bank at the inverter bus have the effect of reducing the short-circuit ratio due to increase in Z_a . However, if a synchronous condenser is also installed in order to deliver some of the required reactive power, this will increase the SCR. To account for these effects, the so-called effective short-circuit ratio (ESCR) is defined by modifying equation (3.3), thus

Table 3.1 Nominal system parameters.

Ac system : $R_a = 14.4$ ohms, $L_{a1} = 26.9$ mH, $L_{a2} = 54$ mH
Ac line : $R_f = 12.0$ ohms, $L_f = 195.0$ mH
Local load : $R_l = 100.0$ ohms, $L_l = 88.0$ mH
Remote load : $R_r = 325.0$ ohms, $L_r = 284.0$ mH
11-th harmonic filter : $R_{11} = 1.0$ ohms, $L_{11} = 50.0$ mH, $C_{11} = 1.163$ μ F
13-th harmonic filter : $R_{13} = 1.0$ ohms, $L_{13} = 53.5$ mH, $C_{13} = 0.778$ μ F
High-pass filter : $R_h = 166.0$ ohms, $L_h = 9.0$ mH, $C_h = 1.504$ μ F
Capacitor bank : $C_c = 17.6$ μ F
New filter : $R_n = 1.0$ ohms, $L_n = 133.0$ mH, $C_n = 13.2$ μ F
Compensation at bus 2 : $C_r = 4.0$ μ F
Dc line : $R_d = 12.0$ ohms, $L_d = 860.0$ mH
Dc smoothing reactors : 0.3 H
Inverter transformer reactance : 16.8 ohms
Effective short-circuit ratio : 3.0
Inverter margin angle : $\gamma = 22$
Nominal operation : 230 kV ac, 500 kV dc, 1000 A dc

$$ESCR = \frac{SCC - Q_{f,c} + Q_{sc}}{P_{dc}} = SCR - \frac{Q_{f,c} + Q_{sc}}{P_{dc}} \quad (3.4)$$

where $Q_{f,c}$ and Q_{sc} denotes the VAR rating of harmonic filters and capacitor bank combined and the synchronous condenser, respectively. The nominal system parameters in Table 3.1 are chosen such that $ESCR = 3.0$. The term “weak” is used to characterize ac systems connected to hvdc inverters with $ESCR$ less than 3.0. A fault occurring in a weak ac system would cause a significant voltage sag on the inverter bus, most likely due to high ac system impedance. In the system model considered above, the $ESCR$ can easily be adjusted by changing Z_a or $Q_{f,c}$.

Characteristic Modes of the Ac System

In order to study the transient behavior of the ac system during a fault, it is useful to look at the characteristic modes of oscillation of the linearized ac network. For example, if a fault occurs at the remote bus in Fig. 3.1 (bus 2), a transient voltage disturbance will be observed at the inverter bus (bus 1). Since the line-to-line voltage at bus 1 is proportional to the commutation voltage at the inverter bridge, the exact transient response of V_1 is critical for the operation of the inverter. If the net commutation voltage drops below a certain threshold value a commutation failure will result. It is therefore important to study the transfer characteristics from bus 2 to bus 1. In the following analysis it is assumed that all faults occur at a remote location (bus 2), since close-up faults or faults at the inverter bus itself would cause an excessive voltage depression and, in most cases, unavoidable commutation failures.

The linearized ac system can be described in general as

$$\frac{dx}{dt} = Ax + Bu \quad (3.5)$$

$$y = Cx \quad (3.6)$$

where the input and output signals, u and y , respectively, are given by

$$u = V_2 \quad (3.7)$$

$$y = V_1 \quad (3.8)$$

The state variables, denoted by x , can be conveniently chosen as inductor currents and capacitor voltages. Thus, referring to Figs. 3.1 and 3.2, x is given by

$$x = [I_{a2} \ I_{a1} \ I_l \ I_{11} \ V_{11} \ I_{13} \ V_{13} \ I_h \ V_h \ I_f \ V_1]^T \quad (3.9)$$

The dynamics of the linearized system can now be written in terms of the state variables given in (3.9), as a set of first order linear differential equations :

$$\frac{dI_{a2}}{dt} = -\frac{R_a}{L_{a2}}I_{a2} + \frac{R_a}{L_{a2}}I_{a1} - \frac{1}{L_{a2}}V_1 \quad (3.10)$$

$$\frac{dI_{a1}}{dt} = \frac{R_a}{L_{a1}}I_{a2} - \frac{R_a}{L_{a1}}I_{a1} \quad (3.11)$$

$$\frac{dI_l}{dt} = -\frac{R_l}{L_l}I_l + \frac{1}{L_l}V_1 \quad (3.12)$$

$$\frac{dI_{11}}{dt} = -\frac{R_{11}}{L_{11}}I_{11} - \frac{1}{L_{11}}V_{11} + \frac{1}{L_{11}}V_1 \quad (3.13)$$

$$\frac{dV_{11}}{dt} = \frac{1}{C_{11}}I_{11} \quad (3.14)$$

$$\frac{dI_{13}}{dt} = -\frac{R_{13}}{L_{13}}I_{13} - \frac{1}{L_{13}}V_{13} + \frac{1}{L_{13}}V_1 \quad (3.15)$$

$$\frac{dV_{13}}{dt} = \frac{1}{C_{13}}I_{13} \quad (3.16)$$

$$\frac{dI_h}{dt} = -\frac{1}{L_h}V_h + \frac{1}{L_h}V_1 \quad (3.17)$$

$$\frac{dV_h}{dt} = \frac{1}{C_h}I_h - \frac{1}{R_h C_h}V_h + \frac{1}{R_h C_h}V_1 \quad (3.18)$$

$$\frac{dI_f}{dt} = -\frac{R_f}{L_f}I_f + \frac{1}{L_f}V_1 - \frac{1}{L_f}V_2 \quad (3.19)$$

$$\frac{dV_1}{dt} = \frac{1}{C_c}I_{a2} - \frac{1}{C_c}I_l - \frac{1}{C_c}I_{11} - \frac{1}{C_c}I_{13} - \frac{1}{C_c}I_h + \frac{1}{R_h C_c}V_h - \frac{1}{C_c}I_f - \frac{1}{R_h C_c}V_1 \quad (3.20)$$

In terms of eqs. (3.5) and (3.6), the system matrix A can be written

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \quad (3.21)$$

where the submatrices A_{11} , A_{12} , A_{21} and A_{22} are given by

$$A_{11} = \begin{bmatrix} -\frac{R_a}{L_{a2}} & \frac{R_a}{L_{a2}^2} & 0 & 0 & 0 \\ \frac{R_a}{L_{a1}} & -\frac{R_a}{L_{a1}^2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_l}{L_l} & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_{11}}{L_{11}} & -\frac{1}{L_{11}} \\ 0 & 0 & 0 & 0 & \frac{1}{C_{11}} \end{bmatrix} \quad (3.22)$$

$$A_{12} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{a2}} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_l} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_{11}} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (3.23)$$

$$A_{21} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_c} & 0 & -\frac{1}{C_c} & -\frac{1}{C_c} & 0 \end{bmatrix} \quad (3.24)$$

$$A_{22} = \begin{bmatrix} -\frac{R_{13}}{L_{13}} & -\frac{1}{L_{13}} & 0 & 0 & 0 & \frac{1}{L_{13}} \\ 0 & \frac{1}{C_{13}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_h} & 0 & \frac{1}{L_h} \\ 0 & 0 & \frac{1}{C_h} & -\frac{1}{R_h C_h} & 0 & \frac{1}{R_h C_h} \\ 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} & \frac{1}{L_f} \\ -\frac{1}{C_c} & 0 & -\frac{1}{C_c} & \frac{1}{R_h C_c} & -\frac{1}{C_c} & -\frac{1}{R_h C_c} \end{bmatrix} \quad (3.25)$$

The input and output vectors, B and C , respectively, are given by

$$B = \left[0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ -\frac{1}{L_f} \ 0 \right]^T \quad (3.26)$$

$$C = [0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1] \quad (3.27)$$

For the nominal circuit parameters specified, the characteristic roots (eigenvalues) of the network were computed using a standard linear analysis program, and are listed below:

$$\lambda_1 = -42.68$$

$$\lambda_2 = -554.12$$

$$\lambda_3 = -980.95$$

$$\lambda_{4,5} = -208.52 \pm j1167.1$$

$$\lambda_{6,7} = -11.80 \pm j4260.9$$

$$\lambda_{8,9} = -12.25 \pm j5019.9$$

$$\lambda_{10,11} = -2171.7 \pm j8709.7$$

In order to determine which of these eigenvalues dominates the network transient response during a fault, it is helpful to evaluate the transfer gain for each characteristic mode. To do this, it is convenient to convert the system equations to modal form by using the transformation

$$x = Mz \quad (3.28)$$

Here, z is a new set of state variables, and the transformation matrix M is the so-called modal matrix given by

$$M = [X_1, X_2, \dots, X_{11}] \quad (3.29)$$

where X_1 through X_{11} are the system eigenvectors. In modal form, the state equations become

$$\frac{dz}{dt} = \Lambda z + B' u \quad (3.30)$$

$$y = C' z \quad (3.31)$$

where

$$\Lambda = \text{diag}(\lambda_1, \lambda_2, \dots, \lambda_{11}) \quad (3.32)$$

$$B' = M^{-1} B \quad (3.33)$$

$$C' = C M \quad (3.34)$$

The transfer gain factor for each mode λ_i is defined as

$$g_i = b'_i c'_i \quad (3.35)$$

where b'_i and c'_i are the i -th elements of B' and C' , respectively. Equation (3.35) was used to calculate the transfer gain for each characteristic mode and the results are listed below:

$$g_1 = 12.82$$

$$g_2 = 59.76$$

$$g_3 = 8.44$$

$$g_{4,5} = 118.11$$

$$g_{6,7} = 1.48$$

$$g_{8,9} = 1.45$$

$$g_{10,11} = 1.45$$

The above results reveal that λ_2 and $\lambda_{4,5}$ are the dominant modes for this case. Therefore, the transient response consists primarily of two components, namely, an exponential term and an underdamped oscillation at about 186 Hz. The exponential term determines the final value of the voltage disturbance due to the fault, after the oscillation dies out. In other words, the exponential determines the magnitude of voltage depression, independent of the network resonant frequencies.

Sensitivity of Eigenvalues to Variation in System Parameters

Since the likelihood of commutation failure in the inverter terminal depends heavily on the transient behavior of the inverter bus voltage, it is important to study how the voltage response can be modified in order to make the inverter valve commutation less sensitive to faults in the ac system. In chapter 2 it was argued that it could be beneficial to increase the dominant mode of oscillation of the inverter bus voltage due to a fault,

Table 3.2 Percentage sensitivity of dominant modes to variation in system parameters.

	Mode 2	Mode 4,5
Ac system	81.4	27.4
Ac line	11.3	9.2
Local load	20.8	2.8
11-th harmonic filter	0.6	3.2
13-th harmonic filter	0.4	2.1
High-pass filter	0.8	3.8
Capacitor bank	10.3	48.9

in order to reduce the likelihood of commutation failure. The question arises, which network parameters are available for change and which parameter variations would be most effective in raising the dominant frequency? To gain insight into this problem, it is useful to look at the sensitivity of the eigenvalues to variation in system parameters.

The sensitivity of λ_i with respect to a parameter p_j , when linearized around a nominal value, can be expressed as

$$S_{p_j}^{\lambda_i} = \frac{\frac{\Delta \lambda_i}{\lambda_{i0}}}{\frac{\Delta p_j}{p_{j0}}} = \left(\frac{\Delta \lambda_i}{\Delta p_j} \right) \left(\frac{p_j}{\lambda_i} \right)_0 \quad (3.36)$$

Based on this definition, the sensitivity of the two dominating modes, λ_2 and $\lambda_{4,5}$, was calculated with respect to variation in ac system parameters, i.e. L_{a1} and L_{a2} , as well as variation in parameters of ac line, local load, harmonic filters and the capacitor bank. The results, expressed in percentages, are summarized in Table 3.2.

The results indicate, that λ_2 is sensitive primarily to the ac system impedance, which may be a fixed system parameter not open to change. This mode is sensitive also, to some extent, to the ac line impedance and the local load, both of which may also be fixed parameters determined by network configuration. On the other hand, the dominant oscillatory component of the transient response, i.e. $\lambda_{4,5}$ is primarily sensitive to the size of the capacitor bank, which is a major design parameter in the system.

Ac System Frequency Spectrum and Transient Response

To gain information on the transfer characteristics of the ac system, from the remote bus (bus 2) to the inverter bus (bus 1), the frequency response of the system was calculated using the nominal system parameters as given in Table 3.1. The transfer gain was measured in terms of the ratio of magnitudes of the bus voltages, i.e. $|V_1|/|V_2|$, and is illustrated in Fig. 3.3. The frequency spectrum exhibits three prominent resonance peaks, namely at around 186 Hz, 678 Hz and 799 Hz, corresponding to eigenvalues $\lambda_{4,5}$, $\lambda_{6,7}$ and $\lambda_{8,9}$, respectively. Of these, the 186 Hz peak is by far the most dominating, which is in accordance with the transfer gain factor $g_{4,5}$, found previously, and which also confirms that $\lambda_{4,5}$ is the dominant oscillatory mode.

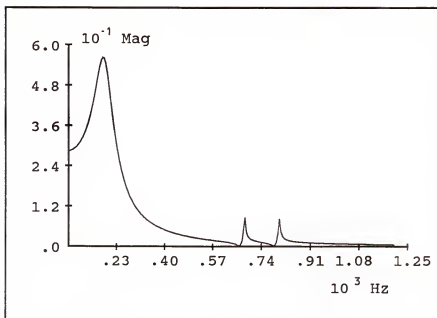


Fig. 3.3 Frequency spectrum of nominal ac network.

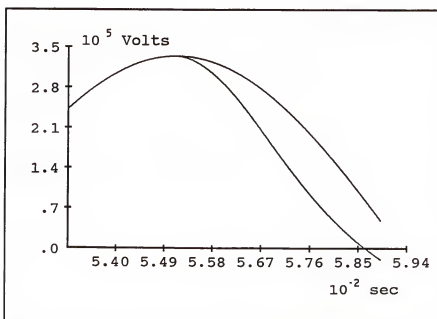


Fig. 3.4 Transient fault response of nominal ac network.

Fig. 3.4 illustrates the transient response of the inverter bus voltage (bus 1) to a three-phase fault at bus 2, again for nominal system parameters. The fault is initiated at the positive peak of the voltage shown. It is easy to observe, that the first swing (dip) of the transient voltage lasts for more than 45° of a fundamental frequency ac wave, which corresponds to a fault condition with a depressed voltage for longer than a typical commutation period. This could easily result in a commutation failure, due mainly to the dominant oscillatory term, if the resulting average commutating voltage is too low. The transient response in Fig. 3.4 is similar to the low frequency transient response illustrated in Fig. 2.15.

Modifying the Network Frequency Spectrum

It is not unusual for the surrounding ac network at an inverter terminal to have a low frequency dominant mode of oscillation as indicated in the previous section. These modes typically lie in the range of 160–220 Hz. Even lower dominant modes have been observed in practice [24]. The frequency analysis of our model system, shown in Fig. 3.1, reveals a dominant frequency at around 186 Hz, and in Fig. 3.4 it is seen that, during a fault, this low frequency mode causes a voltage dip in the inverter bus voltage that last longer than a typical commutation period. This would lead to a commutation failure if the resulting average commutation voltage becomes too low.

By virtue of Fig. 2.16, it would seem beneficial to increase the frequency of the dominant oscillatory response of the network during a fault. The main question is what network parameters can be changed, or what new elements must be added to the network, in order to accomplish this. The likely candidate seems to be the capacitor bank, since the dominant frequency is sensitive to this parameter, as shown in Table 3.2. However, the size of the capacitor bank is usually dictated by voltage and reactive power requirements

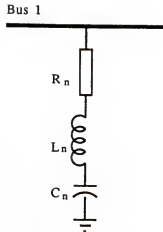


Fig. 3.5 Single tuned harmonic filter.

at the inverter bus. If its size were reduced to increase the dominant resonant frequency, reactive power would have to be supplied from another source. This would probably not be an economically attractive solution for reducing the likelihood of commutation failure. Another possibility is the adjustment of the harmonic filter parameters. However, since the dominant mode frequency is in most realistic cases considerably lower than the filter resonant frequencies, variation of filter parameters is not effective in changing this low frequency characteristic.

From the above discussion, it appears that the only straight-forward way to increase the dominant resonant frequency, without disturbing other important design parameters, is to add a new "filter" to the ac network. One possibility is to supplement the capacitor bank with a simple single-tuned series LC filter, as shown in Fig. 3.5, similar to conventional hvdc harmonic filters, but in this case tuned around the second harmonic. With the new

filter in place, the size of the capacitor bank can be adjusted as before to supply the required amount of fundamental reactive power to the system. With a suitable choice of parameters, the new filter could also supply all the required VARs and thus entirely replace the capacitor bank. The parameters used in this study for the new filter are chosen for the second option, i.e. to replace the filter, and are given in Table 3.1.

For the nominal ac network parameters, and with the new filter included, the eigenvalues of the system were again calculated:

$$\lambda_{1=} - 42.68$$

$$\lambda_{2=} - 526.59$$

$$\lambda_{3=} - 961.89$$

$$\lambda_{4=} - 31345.7$$

$$\lambda_{5,6=} - 34.27 \pm j658.22$$

$$\lambda_{7,8=} - 136.09 \pm j2862.7$$

$$\lambda_{9,10=} - 20.89 \pm j4552.4$$

$$\lambda_{11,12=} - 433.55 \pm j6319.0$$

To determine the dominant modes, the transfer gain was calculated for each eigenvalue as before, with the following results:

$$g_1 = 12.82$$

$$g_2 = 63.52$$

$$g_3 = 9.01$$

$$g_4 = 811.85$$

$$g_{5,6} = 19.13$$

$$g_{7,8} = 114.97$$

$$g_{9,10} = 7.90$$

$$g_{11,12} = 49.98$$

In this case, there are also two dominant characteristic modes during a fault, namely λ_4 and $\lambda_{7,8}$. Therefore, the transient response again consists primarily of two components, i.e. an exponential term as before, and an underdamped oscillation at around 456 Hz. There is also another oscillation about 106 Hz that appears in the transient response to a lesser extent, which corresponds to the mode $\lambda_{5,6}$.

Figs. 3.6 and 3.7 illustrate the relation of the network frequency spectrum and the transient response of the inverter bus voltage to a three-phase fault at bus 2, with the new filter included. This is analogous to Figs. 3.3 and 3.4, except in this case with a higher frequency dominant mode, the transient voltage depression due to the first swing is much less severe, and lasts for a shorter period of time. This should result in a higher net commutating voltage available during a fault. The transient response in Fig. 3.7 corresponds to the ac transient voltage waveform illustrated in Fig. 2.16.

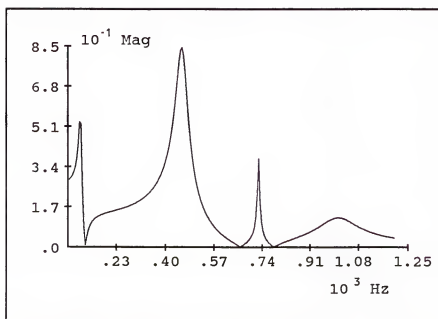


Fig. 3.6 Frequency spectrum of nominal ac network with new filter installed.

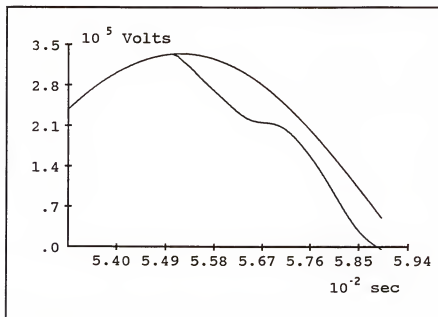


Fig. 3.7 Transient fault response of nominal ac network with new filter installed.

By analyzing the characteristic modes of the linearized ac system it has been shown that during a fault, the transient response of the inverter bus voltage is composed of two main components, corresponding to the two dominant modes. Assuming a three-phase solid fault at the remote bus in Fig. 3.1, a steady-state voltage sag will be observed at the inverter bus, due to the exponential dominant mode. This voltage depression is largely determined by the ac system parameters, which are normally fixed and not open for change. For a very weak ac system ($ESCR = 2.0$ or less), this exponential voltage drop may be sufficient to lower the average commutation voltage to such an extent, that commutation failure will result in any case. In that type of situation the only possible solution would be to somehow increase the strength of the system, for example by installing a synchronous condenser at the inverter bus to supply some of the reactive power needed, or if possible, by simply strengthening the transmission link from the generation site to the inverter bus, and thus reduce the ac system impedance.

The second dominant mode is linked to the resonant frequency of the system. This mode causes the inverter bus voltage to oscillate during a fault, thus having both negative and positive effect on the overall voltage response. During the negative half-wave of the oscillation, the bus voltage will be depressed still further, but during the positive half-wave the overall voltage sag will be less severe. If the frequency of the dominant oscillatory mode is such, that the first positive swing coincides with the next commutation in line after the fault occurs, the average voltage sag during the commutation period may be minimized, and the likelihood of commutation failure reduced significantly.

With the above argument in mind, Fig. 3.4 illustrates the unfavorable effect of a relatively low dominant frequency, in this case in the 180–190 Hz range for our model system in Fig. 3.1, on the transient voltage response. As pointed out earlier,

this frequency range is typical for ac systems connected to hvdc inverter terminals. It is clear from Fig. 3.4, that the first negative half-wave of the oscillatory voltage response in fact coincides with the commutation starting at around 57 ms, which is next in line after the fault occurs. The resulting severe voltage depression during the commutation period is likely to cause a failure. When this is compared to the voltage response illustrated in Fig. 3.7, which incorporates the new filter, we see that due to the increase in the resonance frequency, the first positive half-wave of the voltage oscillation now overlaps the commutation which starts at 57 ms, resulting in a significant increase in the average commutation voltage during the commutation interval. It would therefore seem beneficial to adjust the filter parameters in such a way, that the voltage excursion during the commutation period would be minimized.

It was shown previously, that the transient voltage response is made up of two main components. In case of a persistent fault at the remote bus location, the exponential characteristic mode would cause a permanent voltage drop at the inverter bus. In that case, the inverter bus voltage or commutation voltage would drop to a new steady-state value. This is illustrated in Fig. 3.8 by the dotted curve. The second main component, namely the oscillatory mode, decreases rapidly as determined by its time constant and eventually dies out. However, the effect of this mode on the overall response is crucial during the first few milliseconds after the fault occurs.

In order to gain maximum benefits from the new filter, the dominant oscillatory frequency should be adjusted such that the first positive swing and the next commutation interval will coincide. However, the time of fault occurrence is basically undeterministic, which means that the time interval between the occurrence of the fault and the start of the commutation is a random variable. This interval is shown in Fig. 3.8 and is called the fault angle.

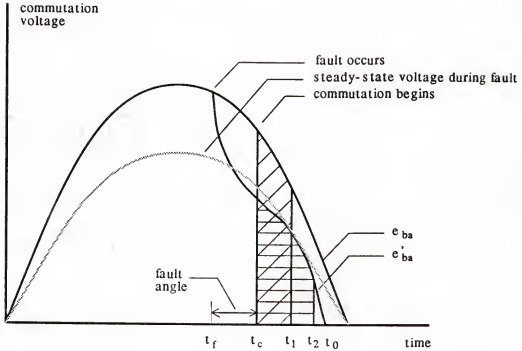


Fig. 3.8 Commutation voltage and definition of fault angle.

Consider a commutation from valve 1 to valve 3 in the model circuit shown in Fig. 2.10. Let us assume that the fault at the remote bus occurs at time t_f and that the commutation starts at time t_c , as shown in Fig. 3.8. The steady-state commutation voltage, denoted by e_{ba} will assume the new transient trajectory e'_{ba} . The voltage depression will cause the commutation interval to increase from $t_1 - t_c$ to $t_2 - t_c$. Any further voltage reduction would push t_2 closer to the voltage zero-crossing indicated by t_0 or even beyond that point, in which case a commutation failure would result. A measure of the likelihood of failure can be expressed as

$$Lf = k \int_{\omega t_c}^{\omega t_2} (e_{ba}(\omega t) - e'_{ba}(\omega t)) d\omega t \quad (3.37)$$

where the integral is evaluated over the commutation period. The fault at the remote bus can be approximately modeled by a step function disturbance. In terms of equations (3.30) and (3.31), this means that the input signal u or the remote bus voltage V_2 is a step voltage and the problem is now to calculate the step response of the linearized system in terms of the output signal y or the inverter bus voltage V_1 . Observing that the transient voltage excursion, $e_{ba} - e'_{ba}$ is proportional to the actual step response, and furthermore, that the fundamental voltage wave e_{ba} varies slowly compared to the transient voltage, we can simply replace the integrand in equation (3.37) by the step response of the linear system.

If we denote the step response as $f(t)$, then an objective function or a cost function can be defined as

$$J(\Delta t) = \int_{t_c}^{t_2} w(t) f(t) dt \quad (3.38)$$

where $w(t)$ denotes a suitable weight function reflecting variable penalty within the integration interval, given by

$$\Delta t = t_2 - t_c \quad (3.39)$$

Let p denote the vector of system parameters chosen as variables for the optimization problem. The objective can now be stated as follows:

$$\min \left\{ J(p, \Delta t) = \int_0^{\Delta t} w(t) f(p, t) dt \right\}, \text{ s.t.} \quad (3.40)$$

$$p_1 \in P_1$$

$$p_2 \in P_2$$

$$\vdots$$

$$p_n \in P_n$$

Here, P_1 through P_n reflect the constraints imposed on the system parameters, denoting the allowable sets of values each parameter can assume.

The step response of the ac system, $f(p, t)$, can be calculated using standard linear control techniques. Based on the modal representation given in equations (3.28) through (3.31), the step response is given by

$$y(t) = C'e^{\Lambda t}z(0) + C' \int_0^t e^{\Lambda \tau} B' u(\tau) d\tau \quad (3.41)$$

where Λ , B' and C' are general system matrices, and may thus represent the system with or without the new filter. Without loss of generality, we can assume that $u(\tau)$ is a unity step input and that the initial conditions, reflected by $z(0)$, are zero. Equation (3.41) can then be expressed as

$$y(t) = f(p, t) = C' \int_0^t e^{\Lambda \tau} B' d\tau \quad (3.42)$$

Since $e^{\Lambda \tau}$ is diagonal, equation (3.42) can be expressed as

$$f(p, t) = \sum_{i=1}^n b'_i c'_i \int_0^t e^{\lambda_i \tau} d\tau \quad (3.43)$$

or

$$f(p, t) = \sum_{i=1}^n \frac{b'_i c'_i}{\lambda_i} (e^{\lambda_i t} - 1) \quad (3.44)$$

where b'_i and c'_i are the elements of B' and C' , respectively. As expected, equation (3.44) shows that the response of the system is the weighted sum of the individual modes of the system, as stated by classical control theory.

To evaluate the cost function given in equation (3.38), a standard numerical integration technique like Simpson's rule can be used. The remaining task is then to minimize the cost subject to the given set of constraints, as stated in equation (3.40). Since $J(p, t)$ is a scalar field, a search technique based on the gradient can be used, for example the *best-step steepest descent* technique. The method requires an initial "guess" of p , say p^0 and an evaluation of $J(p^0) = J^0$. The computation sequence is then given by

$$p^{k+1} = p^k + \Delta\tau I q|_{p=p^k} \quad (3.45)$$

where q is the gradient of J , $\Delta\tau$ is the iteration step length in direction of q and I is the identity matrix.

Since J is evaluated numerically the gradient takes the discrete form

$$q = (q_1, q_2, \dots, q_n)^T \quad (3.46)$$

where the i^{th} element is

$$q_i = \frac{J(p + \Delta p_i) - J(p)}{\Delta p_i} \quad (3.47)$$

and $\Delta p_i = (0, 0, \dots, 0, \delta, 0, \dots, 0)$, with δ in the i^{th} position.

In the best-step steepest descent (ascent) search, because of the computations involved in evaluating the gradient at a given point, the search in the direction of the gradient is continued until

$$\frac{\Delta J(p^k + \Delta \tau q(p^k))}{\Delta(\Delta \tau)} < \epsilon \quad (3.48)$$

for some $\Delta \tau$, to make the most of each gradient computation. The overall search is continued until

$$\|q(p^k)\| < \epsilon \quad (3.49)$$

or until p^k hits constraint boundaries. In the latter case an appropriate step is taken away from the constraint boundaries perpendicular to the gradient, and the search is resumed in the gradient direction.

Optimal Choice of Single-Tuned Filter

The simplest type of filter available for the purpose of modifying the ac network frequency response is the single-tuned harmonic filter depicted in Fig. 3.6. It was shown

previously in this chapter that this type of filter is indeed effective in raising the frequency of the dominant mode of oscillation, as illustrated in Fig. 3.5. In this section it is shown, how the filter parameters can be adjusted to yield optimum performance of the filter, with respect to minimizing the likelihood of commutation failures.

Of the three circuit elements of the filter, only the inductance and the capacitance are important with respect to optimization, since the resistance is normally small. For the filter shown in Fig. 3.6 the resonant frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_n C_n}} \quad (3.50)$$

The reactive power compensation at 60 Hz is required to equal that of the capacitor bank, which the filter replaces. This can be expressed as

$$120\pi L_n - \frac{1}{120\pi C_n} = \frac{-1}{120\pi C_c} \quad (3.51)$$

where C_c represents the size of the capacitor bank. This puts a constraint on the parameter choice and reduces the optimization in fact to a one dimensional problem. This can be seen when equations (3.50) and (3.51) are solved together to give

$$C_n = C_c \left[1 - \left(\frac{60}{f_0} \right)^2 \right] \quad (3.52)$$

and equation (3.50) is rewritten as

$$L_n = \frac{1}{(2\pi f_0)^2 C_n} \quad (3.53)$$

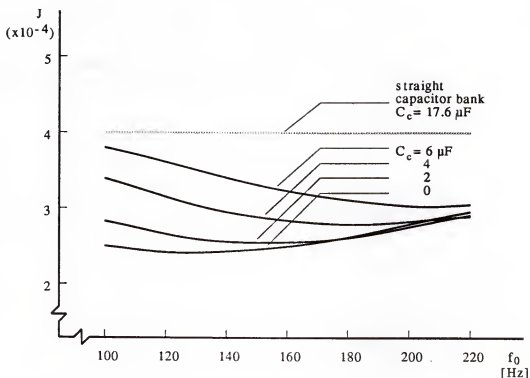


Fig. 3.9 Optimum frequency for single-tuned filter, with type I weight function.

The frequency f_0 of the tuned filter can therefore serve as the single argument of the objective function, as defined in the previous section, since both C_n and L_n are determined by the resonant frequency at fixed compensation by equations (3.52) and (3.53), respectively.

Based on the above argument the objective function was calculated according to equation (3.38), with both the capacitor bank and the new filter connected simultaneously

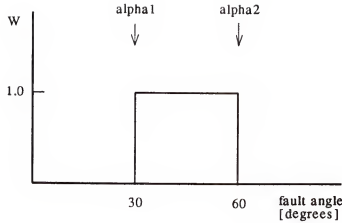


Fig. 3.10 Weight function type I.

at the inverter bus. The calculations were repeated for different sizes of capacitor banks and the filter parameters were adjusted in each case such that the total VAR requirements were satisfied. The results are illustrated in Fig. 3.9. For the system parameters used, the total reactive power demand corresponded to a capacitor size of $17.6 \mu\text{F}$, as indicated in Fig. 3.9 by the dotted line, which denotes the value of the cost function when a straight capacitor bank is used, and is displayed in the figure merely as a reference level. The weight function used for this computation is shown in Fig. 3.10 (type I). The cost function was calculated for each value of filter resonant frequency f_0 , by integrating the step response of the inverter bus voltage for fault angles between 30° and 60° , as determined by the weight function in Fig. 3.10.

The random character of the fault angle is reflected in the choice of weight function. Small fault angles indicate that the commutation of the valve-pair under consideration

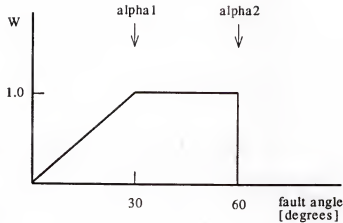


Fig. 3.11 Weight function type II.

starts soon after the occurrence of the fault, and it is not likely that the commutation voltage will be severely affected before commutation is completed. This is reflected in the weight function by ignoring fault angles less than 30° . Likewise, if the commutation angle is large, indicating that the fault occurs timely before the start of the commutation, the control system of the hvdc inverter terminal will probably have enough lead time to advance the firing pulse to counter the voltage dip and prevent failure. Based on a typical response time of the inverter control, fault angles larger than 60° are consequently also ignored, as reflected by the weight function.

The results in Fig. 3.9 indicate that the cost function is smallest when the capacitor bank is replaced entirely by the new filter. In that case, and with the given weight function, the cost has a minimum value of $2.4 \times (10^{-4})$ for a filter resonance frequency at around 130 Hz. As the capacitor size increases so does the cost. With the straight

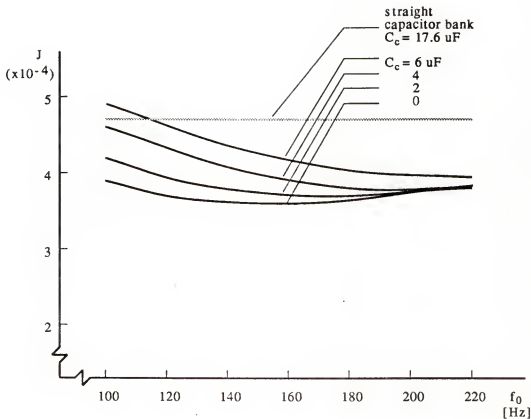


Fig. 3.12 Optimum frequency for single-tuned filter, with type II weight function.

capacitor bank connected at the inverter bus, the cost is approximately 4.0×10^{-4} , which is larger than the cost for any combination of filter and capacitor bank or filter alone.

A modified version of the weight function (type II) is illustrated in Fig. 3.11. In this case the gradual increase in the importance of the fault angle between 0° and 30° is reflected in the linear ramp for that interval. With this type of weight function the objective in equation (3.38) was again calculated, and the results are shown in Fig. 3.12.

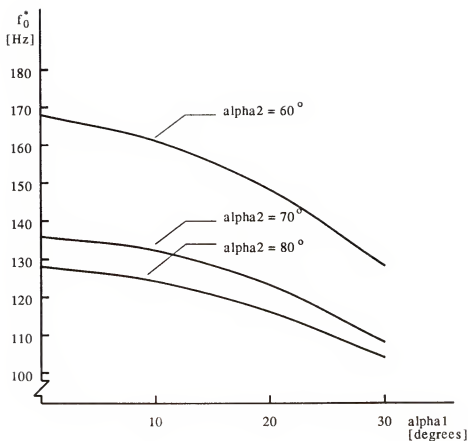


Fig 3.13 Effect of weight function (type I) parameters on optimum filter frequency.

The results are similar to those in Fig. 3.9, with the cost being smallest when the new filter replaces the capacitor bank, and with highest cost when a straight capacitor bank is used. The most interesting feature in the results shown in Fig. 3.12 is the shift of the minimum cost to a higher resonance frequency of around 155 Hz instead of 130 Hz before. However, this may have a minor effect on the overall likelihood of commutation failures, since the minimum is very broad, with only a small difference in cost for frequencies in the 130–155 Hz range. Compared to the straight capacitor case however,

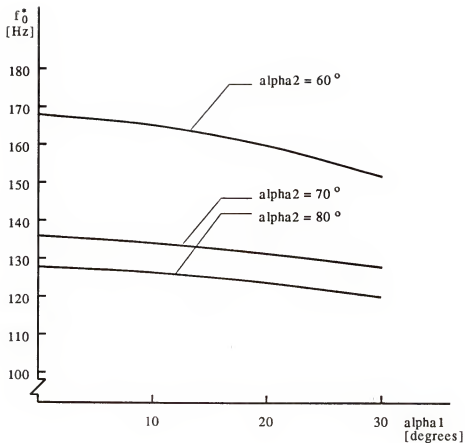


Fig 3.14 Effect of weight function (type II) parameters on optimum filter frequency.

there is a significant reduction in cost with the new filter installed for both types of weight functions. It should be noted, that since the weight function of type II extends the lower limit of integration down to a fault angle of 0° , as compared to 30° for type I weight function, all cost values in Fig. 3.12 are higher than corresponding values in Fig. 3.9.

To further investigate the shift in optimum frequency observed in Fig. 3.12 compared to Fig. 3.9, a repeated calculation of the objective was performed, in which the weight functions were gradually modified by varying the parameters α_1 and α_2 , shown in Figs.

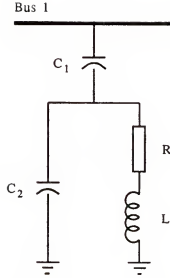


Fig 3.15 Double-tuned filter.

3.10 and 3.11. The results of these calculations are illustrated in Figs. 3.13 and 3.14 for weight functions of type I and type II, respectively. The graphs show how the optimum frequency f_o^* varies as the weight function parameters are changed. The results for the particular case when $\alpha_1 = 30^\circ$ and $\alpha_2 = 60^\circ$ are the same as shown in Figs. 3.9 and 3.12, for $C_c = 0$, or around 130 Hz and 155 Hz, respectively.

Alternate Filter Design

Fig. 3.15 illustrates an alternative filter type that can be installed to replace the capacitor bank at the inverter bus, in order to increase the frequency of the dominant oscillatory mode of the ac system. This type of filter has two resonance frequencies and is consequently called a double-tuned filter. Assuming that the resistance R is small, the series resonance frequency is approximately given by

Table 3.3 Parameters for double-tuned filter.

$R = 1.0 \text{ ohm}$
$L = 133.0 \text{ mH}$
$C_1 = 13.2 \text{ uF}$
$C_2 = 1.0 \text{ uF}$

$$f_s \approx \frac{1}{2\pi\sqrt{L(C_1 + C_2)}} \quad (3.54)$$

Similarly, the shunt or parallel resonance frequency is approximately determined by

$$f_p \approx \frac{1}{2\pi\sqrt{LC_2}} \quad (3.55)$$

To replace the capacitor bank, the double-tuned filter must supply the reactive power needed at 60 Hz. This can be expressed as

$$\frac{1}{C_c} \approx \frac{1 - (120\pi)^2 L (C_1 + C_2)}{C_1 (1 - (120\pi)^2 LC_2)} \quad (3.56)$$

where C_c denotes the size of capacitor bank. It should be noted that in the limit, for a small value of C_2 , this type of filter simply reduces to the single-tuned filter considered

earlier. The values for the filter parameters used in this study are given in Table 3.3. It should be noted that this is not an “optimal” set of values, but they are used here as starting values later to be optimized.

For ac system parameters as given in Table 3.1 and the double-tuned filter connected at the inverter bus, the eigenvalues of the system were once again calculated, as listed below:

$$\lambda_1 = -42.68$$

$$\lambda_2 = -526.90$$

$$\lambda_3 = -962.44$$

$$\lambda_{4,5} = -31.08 \pm j643.96$$

$$\lambda_{6,7} = -155.14 \pm j2668.4$$

$$\lambda_{8,9} = -20.87 \pm j4521.02$$

$$\lambda_{10,11} = -262.21 \pm j6021.8$$

$$\lambda_{12,13} = -5030.7 \pm j15075$$

As in previous cases, there are two dominant modes: an exponential mode represented by λ_2 , and an oscillatory mode $\lambda_{6,7}$, with a resonance frequency of around 425 Hz. The frequency spectrum of the ac system with this filter is shown in Fig. 3.16, and the transient response of the inverter bus voltage to a remote three-phase fault is illustrated in Fig. 3.17. As expected, with the dominant frequency close to that of the single-tuned filter considered earlier and the value of C_2 relatively small, both the frequency spectrum and the transient response are very similar to that of the single-tuned filter, as shown in Figs. 3.6 and 3.7.

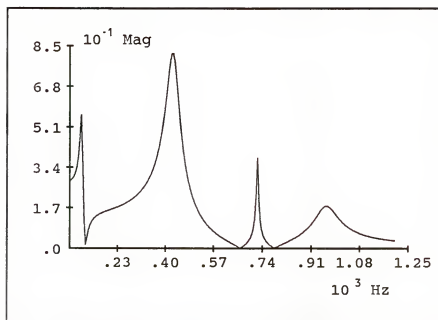


Fig. 3.16 Frequency spectrum of nominal ac network with double-tuned filter installed.

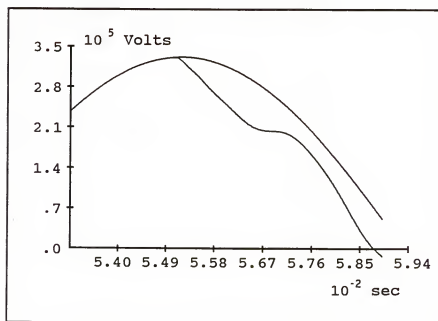


Fig. 3.17 Transient fault response of nominal ac network with double-tuned filter installed.

Although the filter described above contains three variables that can be adjusted independently, i.e. L , C_1 and C_2 , the VAr requirement imposes a constraint and reduces the degree of freedom to two variables. For the purpose of optimization therefore, a convenient choice of variables is to simply use the two resonance frequencies f_s and f_p . This is tantamount to using two of the three filter parameters, i.e. C_1 and C_2 , in the optimization, with one parameter, i.e. L , dependent. Equation (3.56) can be rewritten as

$$C_1 \approx C_c \left(\frac{1 - \left(\frac{60}{f_s}\right)^2}{1 - \left(\frac{60}{f_p}\right)^2} \right) \quad (3.57)$$

and equations (3.54) and (3.55) may be solved together to give

$$C_2 \approx C_1 \left(\frac{\left(\frac{f_s}{f_p}\right)^2}{1 - \left(\frac{f_s}{f_p}\right)^2} \right) \quad (3.58)$$

Finally, L can be calculated from equation (3.54) as

$$L \approx \frac{1}{(2\pi f_s)^2 (C_1 + C_2)} \quad (3.59)$$

Equations (3.57) through (3.59) may be used in the optimization of the filter, as an algorithm to calculate the circuit parameters for any given set of resonant frequencies and for a predetermined capacitor bank size.

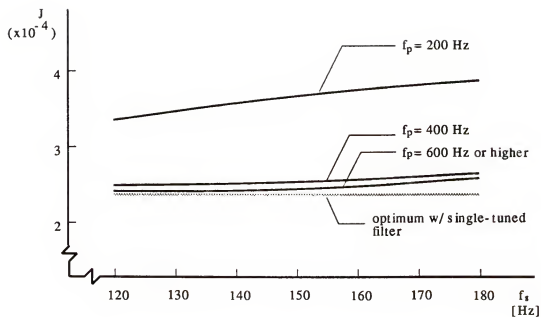


Fig. 3.18 Optimum frequencies for double-tuned filter, with type I weight function.

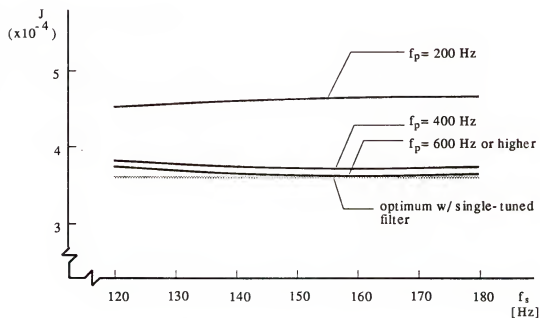


Fig. 3.19 Optimum frequencies for double-tuned filter, with type II weight function.

The cost function for the double-tuned filter was calculated based on the definition in equation (3.38), as a second order scalar field, with the two resonance frequencies f_s and f_p as parameters, and with the help of equations (3.57) through (3.59). The results are illustrated in Figs. 3.18 and 3.19 for weight functions of type I and type II, respectively. The basic results for both cases are the same. The filter performs better as the parallel resonance frequency increases, which is equivalent to reducing the size of C_2 according to equation (3.55), since L is essentially determined by C_1 and f_s only, when C_2 is small. As mentioned earlier, in the limit when C_2 assumes very small values, the filter simply reduces to the single-tuned filter considered earlier. The results indicate that for f_p higher than approximately 600 Hz, no further major improvements are observed in the cost function. For higher frequencies, the effect of C_2 becomes insignificant and the minimum cost approaches the optimum results found in the case of the single-tuned filter, as indicated by the dotted lines, which are shown here for reference only. It must therefore be concluded that the double-tuned filter will not yield any improvements, in terms of reduced likelihood of commutation failures, over the single-tuned filter considered earlier, but imposes of course additional monetary cost due to the capacitor C_2 . In the limit case, i.e. for f_p higher than approximately 600 Hz, the optimum value of series resonance frequency is essentially the same as found earlier for the single-tuned filter or around 130 Hz and 155 Hz respectively, for weight functions of type I and type II. This can be seen by comparison with Figs. 3.9 and 3.12.

Effect of Fifth- and Seventh-Harmonic Filters

Harmonic frequencies are generated as biproduct in all systems that apply switching circuits, including hvdc converter terminals. The first commercial hvdc systems almost exclusively used 6-pulse mercury-valve circuits for rectification and inversion. In this type of converters, the most prominent harmonic frequencies on the ac side of the

converter are the 5-th and the 7-th harmonics, and on the dc side the 6-th harmonic. Eventually, some of these early converters were later upgraded to 12-pulse systems, by series connecting two 6-pulse circuits, primarily to increase transmission capacity and the efficiency of the transmission link. In the 12-pulse converters the dominating harmonic frequencies are the 11-th and the 13-th on the ac side and the 12-th on the dc side, whereas the 5-th and the 7-th harmonics are less important. In many cases however, the upgraded systems still apply 5-th and 7-th harmonic filters, in addition to the 11-th and 13-th harmonic filters and the broadband high-pass filter shown in Fig. 3.2.

In order to study the effect the lower-order filters may have on the frequency spectrum and the transient fault characteristics of ac systems, 5-th and 7-th harmonic filters were added to the basic ac system configuration illustrated in Figs. 3.1 and 3.2. To account for the added contribution of the the harmonic filters in terms of reactive power generation, the size of the capacitor bank was adjusted accordingly. The actual parameters used are given in Table 3.4.

Table 3.4 Parameters for 5-th and 7-th harmonic filters, and capacitor bank.

$R_5 = 1.0 \text{ ohm}$
$L_5 = 93.8 \text{ mH}$
$C_5 = 3.0 \text{ uF}$
$R_7 = 1.0 \text{ ohm}$
$L_7 = 47.9 \text{ mH}$
$C_7 = 3.0 \text{ uF}$
$C_c = 11.4 \text{ uF}$

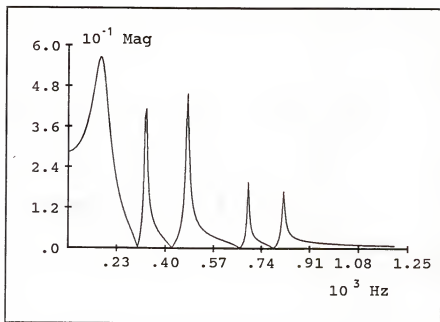


Fig. 3.20 Frequency spectrum of nominal ac network with 5-th and 7-th harmonic filters installed.

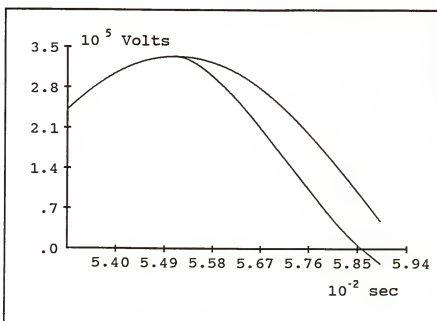


Fig. 3.21 Transient fault response of nominal ac network with 5-th and 7-th harmonic filters installed.

With the 5-th and the 7-th harmonic filters connected at the inverter bus, the frequency spectrum of the ac system and the transient commutation voltage were computed, and the results are illustrated in Figs. 3.20 and 3.21, respectively.

The frequency spectrum in Fig. 3.20 illustrates a dominant oscillatory mode at around 165 Hz, which is 20 Hz lower than the dominant mode for the basic system configuration, without the 5-th and the 7-th harmonic filters and the new filter, as shown in Fig. 3.3. This is due to the proximity of the frequencies of the low-order filters to the dominant frequency peak. The effect of these filters is indicated by the additional resonant peaks at 320 Hz and 470 Hz, and the effect of the 11-th and the 13-th harmonic filters is seen at 680 Hz and 810 Hz. All of these however, are of minor consequence, since the transfer gain associated with them is low. This is confirmed by the transient fault response shown in Fig. 3.21, which does not contain any significant high-frequency oscillations. In fact, the response resembles that of the basic system configuration, shown in Fig. 3.4. The negative voltage excursion is at its peak during the time period where commutation is most likely to occur and, consequently, the likelihood of commutation failure would be relatively high, similar to that of the basic system.

In the previous sections the effect and the optimization of the proposed new filter was based on the assumption that the ac system had only the 11-th and the 13-th harmonic filters connected at the inverter bus. As pointed out, this is a normal configuration for a modern 12-pulse hvdc system. Fig. 3.20 shows that the 5-th and the 7-th harmonic filters influence the frequency response of the ac system mainly in the 300–500 Hz range. As indicated in Fig. 3.6, the dominant oscillatory mode due to the effect of the new filter also is located in this frequency range. It can therefore be expected, that the 5-th and the 7-th harmonic filters will to some extent limit the effectiveness of the new filter

or alter the optimization scheme. In order to evaluate the net effect however, a further study is required.

Conclusion

Commutation failures are frequently experienced in the operation of hvdc inverter terminals. The problem becomes more significant if the inverter is connected to a weak ac system. In this chapter, a realistic model of such a system has been studied, in particular the relation between the frequency spectrum of the system and the transient fault response of the inverter bus voltage.

When relatively small fault disturbances are considered, the transient response of the ac system is entirely determined by the characteristic modes (eigenvalues) of the linearized system. In this chapter it has been shown, that the dominant modes can have a major impact on the likelihood of commutation failure in the inverter bridge. By increasing the frequency of the dominant oscillatory mode, the net commutation voltage during the fault period can be increased significantly, which has the effect of reducing the likelihood of commutation failure.

In this chapter it was found, that the capacitor bank, which is normally installed for reactive power compensation at the inverter bus, has a crucial effect on the frequency spectrum of the system. The frequency of the dominant mode can be increased by replacing the capacitor bank with a single tuned filter, similar to the harmonic filters, but tuned at around 130–155 Hz and supplying equal amount of VARs at 60 Hz as the capacitor bank. The frequency characteristics of the filter can be adjusted such that the voltage drop due to the fault is minimized during the commutation period.

To evaluate the benefits of the new filter over the straight capacitor bank, in terms of reduced likelihood of commutation failures, a cost function was defined, that measures

the voltage excursion on the inverter bus during a fault. Numerical evaluation of the cost function shows, that the new filter offers a reduction in "cost" in the range of 30–40%, when measured over a specified fault angle range. In order to translate this cost reduction into a potential reduction in the likelihood of commutation failures, and thus to verify the benefits of the new filter, a computer simulation of the system must be performed.

CHAPTER 4

HVDC SYSTEM SIMULATION

Introduction

In the previous chapter it was theorized that the likelihood of commutation failure in an hvdc inverter, due to faults in the adjoining ac system, could be reduced by increasing the frequency of the dominant oscillatory mode of the ac system transient response. In order to test the observations made and to evaluate the benefits of modifying the ac network frequency spectrum for a variety of conditions, a computer simulation was set up for an hvdc system, using EMTP (ElectroMagnetic Transients Program).

The simulation tests were centered around the commutation of a particular valve pair in the inverter bridge. To induce commutation failure, the inverter bus voltage was suppressed by applying various types of ac system faults of different severity at a remote bus location. The performance of the system was observed, both with fixed inverter controls, i.e. without advancing the firing angle due to the voltage sag, and with the full controls activated.

Commutation failure is to some extent a statistical phenomenon which depends on random events, such as the time of occurrence of fault. Thus to get a measure of the likelihood of failure, multiple simulation tests were performed, as the time of fault was varied relative to the gating pulses at the inverter. Comparisons were made between the use of a straight capacitor bank and the proposed new filter to increase the low-frequency resonance. The present chapter gives a detailed account of the results obtained from these simulation tests.

Computer Simulation Test Model

The computer simulation was set up for an hvdc system using EMTP (ElectroMagnetic Transients Program). A two-terminal system with twelve-pulse rectifier and inverter circuits was modeled in detail. The inverter is connected to a typical three-phase ac network as modeled in Fig. 3.1. The inverter is supplied by a rectifier through a monopolar dc line. During normal operation the rectifier regulates the current in constant current mode while the inverter regulates voltage with a predictive constant extinction angle control. Both rectifier and inverter valves and control pulses are represented individually to allow for study of commutation failures. The ac source-behind-impedance can be adjusted to represent a weak ac system. The remote load bus (bus 2) may be short-circuited to represent a fault of varying severity, in order to suppress the inverter bus voltage and cause commutation failure. The ac network also includes eleventh, thirteenth and high-pass harmonic filters and provision for a straight capacitor bank or the proposed new filter. More detailed information on the simulation model is given in Appendix A, which contains a complete listing of a typical EMTP datafile for simulation of a two-terminal system, and in Appendix B in the form of schematic diagrams.

Simulation Study

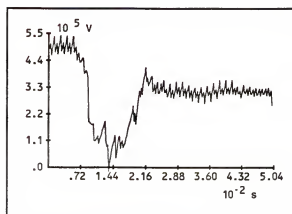
Simulation tests were performed to induce commutation failure during various types of faults at the remote bus (bus 2 in Fig. 3.1), including solid three-phase to ground fault, line-to-line and single-phase to ground faults. The nominal system parameters chosen for the simulation illustrate the effect of suppressing the inverter bus voltage by a range of approximately 25% to 40% during a three-phase fault. The effective short circuit ratio (ESCR) of the system ranged from 2.0 to 3.0.

Fig. 4.1 shows the transient fault response of the nominal system to a three-phase fault, with the straight capacitor bank connected at the inverter bus. The ac system has ESCR of 3.0 and the inverter is operated at a constant gamma of 22° . Under these conditions the ac network has the frequency spectrum and transient response shown in Figs. 3.3 and 3.4, respectively, as discussed in chapter 3. The waveforms in Fig. 4.1 represent, respectively from above, the direct voltage at the inverter, the direct current and the ac voltages at the inverter bus. The occurrence of a commutation failure due to the fault, which is applied at 5.3 ms simulation time, can be clearly observed from the waveforms.

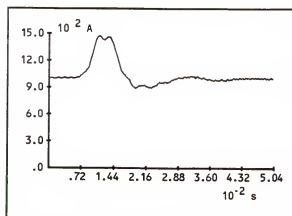
Figs. 4.2 and 4.3 illustrate the transient fault response of the system in a similar fashion for two different cases, again due to a three-phase fault. Fig. 4.2 shows the response of a weaker system with $ESCR = 2.0$, whereas the waveforms in Fig. 4.3 show the response when the inverter is operating at a smaller gamma of 18° . Finally, in Fig. 4.4, the effect of an unsymmetrical fault is illustrated, in this case a line-to-line fault between a and b phases on the remote bus, for the base system configuration.

Effect of New Filter

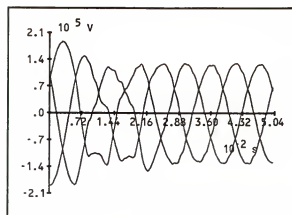
The simulation tests illustrated in the previous section were repeated as the capacitor bank at the inverter bus was replaced by a single-tuned harmonic filter. The filter, which is depicted in Fig. 3.5, was tuned to 160 Hz. Otherwise, the system conditions were the same and the fault was applied in each case at the same time as before, i.e. at 5.3 ms simulation time. The results of these tests are illustrated in Figs. 4.5 through 4.8, respectively for the base case with $ESCR = 3.0$ and $\gamma = 22^\circ$, for a weak system with $ESCR = 2.0$, for $\gamma = 18^\circ$, all subject to a three-phase fault, and for a line-to-line fault in the base system. The ac network has the frequency spectrum and transient response shown in Figs. 3.6 and 3.7 in the base configuration.



(a)

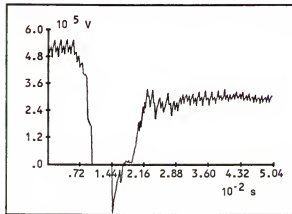


(b)

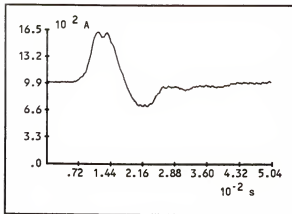


(c)

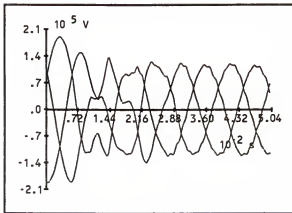
Fig. 4.1 Transient fault response of base system with capacitor bank; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).



(a)

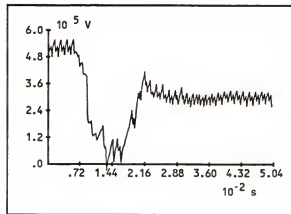


(b)

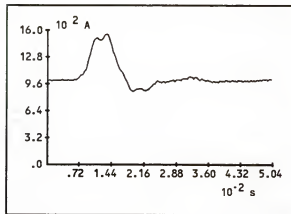


(c)

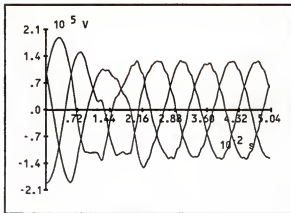
Fig. 4.2 Transient fault response of system with $ESCR = 2.0$; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).



(a)

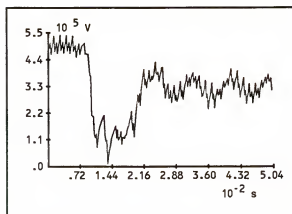


(b)

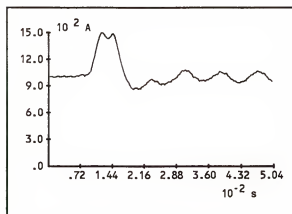


(c)

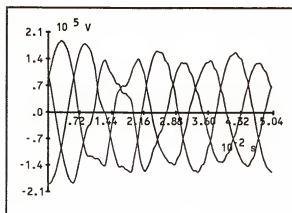
Fig. 4.3 Transient fault response of system with $\gamma = 18^\circ$; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).



(a)

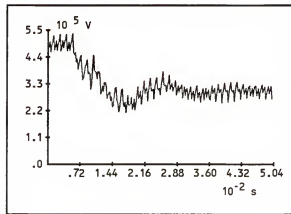


(b)

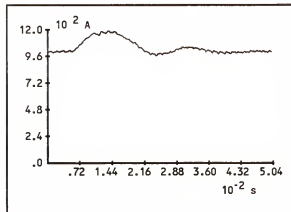


(c)

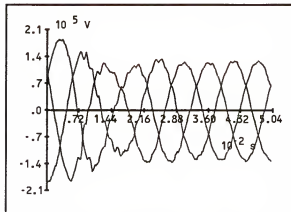
Fig. 4.4 Transient fault response of base system to a line-to-line fault; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).



(a)

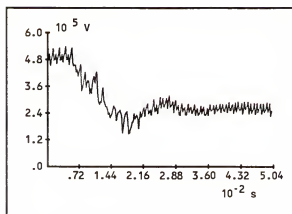


(b)

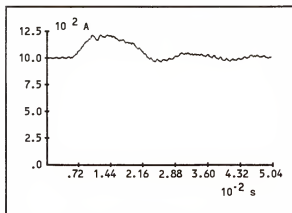


(c)

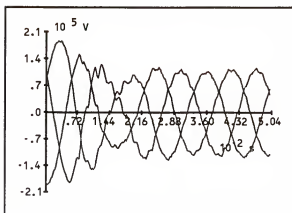
Fig. 4.5 Transient fault response of base system with new filter; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).



(a)

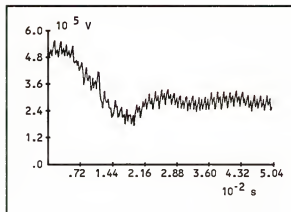


(b)

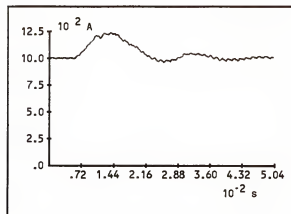


(c)

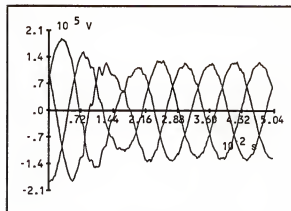
Fig. 4.6 Transient fault response of system with new filter and ESCR = 2.0; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).



(a)

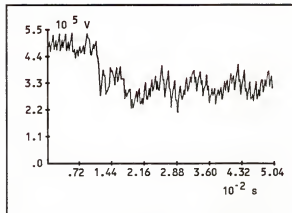


(b)

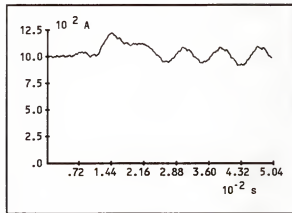


(c)

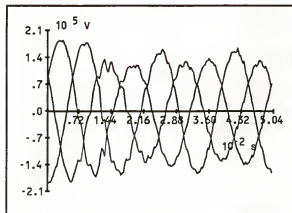
Fig. 4.7 Transient fault response of system with new filter and $\gamma = 18^\circ$; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).



(a)



(b)



(c)

Fig. 4.8 Transient fault response of system with new filter to a line-to-line fault; inverter direct voltage (a), direct current (b), inverter bus ac voltages (c).

It is clear from Figs. 4.5–4.8, that commutation failure has been prevented in all cases, under the same condition as illustrated in the previous section, by changing the ac network dominant frequency.

Likelihood of Failure with Fixed Inverter Control

Figs. 4.1 through 4.8 typify the transient response of the nominal system, with and without the new filter connected at the inverter bus. In all of the above cases the ac system fault at the remote bus was imposed at a fixed time instant during the simulation, namely at 5.3 ms simulation time. Commutation failure, however, is a statistical phenomenon which depends on random events, such as the time of occurrence of the fault. Therefore, to get a measure of the likelihood of failure, multiple simulations were performed, as the time of fault was varied relative to the gating pulses at the inverter.

As before, the inverter bus voltage was suppressed to induce commutation failure, by applying various types of faults at the remote load bus. During normal operation, commutation occurs every 30° within the 60 Hz period. Thus, to limit the volume of data, the multiple simulation tests were focused on the commutation process of a particular valve-pair in the inverter bridge. This is also justified due to the symmetry of the inverter bridge, as the commutation of any valve-pair can be considered to represent the performance of the inverter as a whole. The fault angle, which measures the time between the occurrence of the fault and the start of commutation, is therefore applicable only to the valve-pair being observed in the multiple tests.

In order to independently explore the effects of various system parameters, initial studies were made with the inverter control held fixed so that the gate pulses were frequency-locked to the prefault ac network conditions. The simulation test model includes a predictive type inverter control, which maintains a constant extinction angle γ

during normal operation of the two-terminal system. This means that the inverter controls the voltage on the dc link, whereas the rectifier is in constant current control. As the voltage starts to sag on the inverter bus due to a fault, the voltage measuring circuits of the inverter pick up the trend and the inverter firing angle is advanced before the start of the next commutation in line, in order to compensate for the volt-seconds lost due to the disturbance. A similar course of action is taken in the case of a sudden direct current increase. With the inverter control held fixed, this would tend to give pessimistic results for faults occurring significantly ahead of a gate pulse, since the control is not allowed to advance the firing time.

Fig. 4.9 shows graphically a record of commutation failures observed during commutation of the particular valve-pair chosen for the test, as a function of fault angle, when a solid three-phase fault to ground was applied at the remote bus. Again, the fault angle measures the time interval, on a 60 Hz basis, from the initiation of the fault until the gate time of the specified valve-pair for which the commutation process is being observed. Thus, a fault angle of 0° means the fault occurs exactly at the instant when commutation begins. The fault was initiated at equally spaced time instants corresponding to a 5° increment in the fault angle. The test interval was chosen for fault angles between 0° and 60° , based on a typical response time of the inverter control circuit. This is also in accordance with the weight functions chosen for filter optimization purposes in chapter 3.

In the results shown here for the base case, for which the effective short circuit ratio (ESCR) was approximately 3.0 and the inverter was operated at a constant extinction angle γ of 22° , the simulated fault suppressed the inverter bus voltage by about 30% during the fault. The other test cases shown represent more severe conditions that increase the likelihood of failure. These include a weaker system with $\text{ESCR} = 2.0$ and a case in which the fault occurs 30% closer to the inverter bus. In both of these test cases

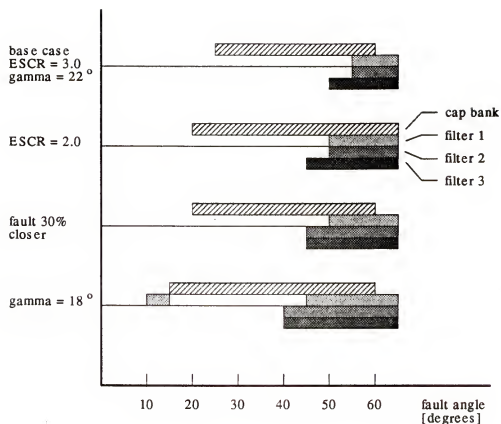


Fig. 4.9 Commutation failures in a specified valve-pair with fixed inverter control and three-phase fault.

the inverter bus voltage was suppressed an additional 5–10% compared to the base case. In the last test the inverter extinction angle was lowered to 18° .

The main objective of the multiple simulation test was to compare the performance of the new filter to that of a straight capacitor bank. Optimization results in chapter 3 suggest, that the actual tuning of the filter, which is of the single-tuned type illustrated in Fig. 3.5, is not critical, as the objective function curves portray a rather broad minimum. Therefore, to test this, the filter was adjusted to three different center frequencies, i.e. 120 Hz, 140 Hz and 160 Hz, corresponding to filters 1, 2 and 3, respectively. Each test case therefore, includes four different system configurations.

Looking at the first test case in Fig. 4.9, i.e. the base case, we can see that when the straight capacitor bank is connected at the inverter bus, the first commutation failure occurs when the fault angle reaches approximately 25° . This corresponds to the fault occurring around 1.16 ms prior to the start of the commutation. However, the last failure is observed at 55° . Due to the discrete character of the tests, with 5° increments in the fault angle, the last failure of the capacitor bank is in fact shown to end at 60° . Similarly, when the new filter is connected, the last commutation failure is actually observed at 60° , but the graph is extended to 65° . Thus for filter 1, only two failures were observed, namely at 55° and 60° .

The results in Fig. 4.9 show, that as the severity of the fault increases and the effect on the inverter bus voltage becomes more adverse, commutation failures occur more frequently in the specified fault angle interval. However, with the new filter in place, it is observed that the commutation failures for the given valve-pair are consistently delayed by approximately 25–30°, depending on the actual tuning of the filter.

In order to quantify the results observed in Fig. 4.9, we can conveniently define the likelihood of failure as the ratio of accumulative fault angle interval in which commutation

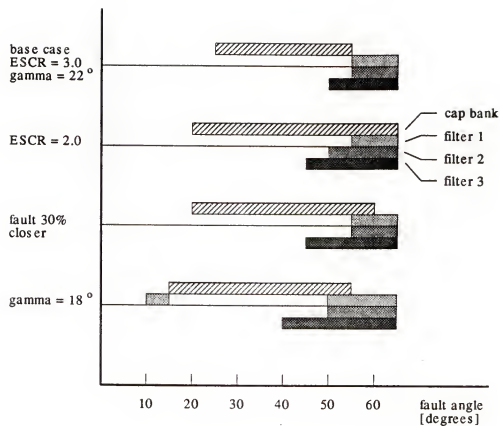


Fig. 4.10 Commutation failures in a specified valve-pair with fixed inverter control and line-to-line fault.

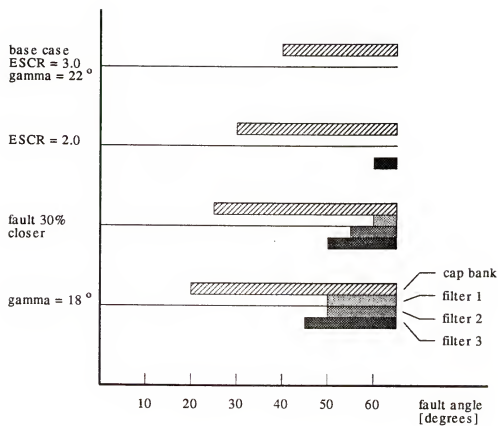


Fig. 4.11 Commutation failures in a specified valve-pair with fixed inverter control and single-phase fault.

failures are observed, to the total interval tested. Based on this definition, we can conclude that, for the given test interval of fault angles, the likelihood of failure is drastically reduced by the application of the new filter, regardless of the actual filter frequency chosen in the 120–160 Hz range. However, with the inverter controls being held fixed, as the fault angle increases, commutation failure would eventually occur due to the steady-state decrease in the inverter bus voltage. Thus, if the probability of failure was considered in the absolute sense, the new filter would not help the situation in case of fixed controls. Rather, the principal benefit of the filter is a delaying action which, in a more realistic setting, would allow the inverter control additional lead time to act to prevent failure.

Additional simulations were performed to investigate the effect of different types of faults. Thus, Figs. 4.10 and 4.11 illustrate the recorded commutation failures in the case of a line-to-line fault and a single-phase to ground fault respectively, applied at the remote bus. The simulation procedure was otherwise the same as described above. The results of these tests are similar to those found when a three-phase fault was applied, in that commutation failures are consistently delayed when the new filter is connected in replacement for the straight capacitor bank. The likelihood of failure however, is decreased when these unbalanced types of faults occur. Thus for the base case and a single-phase fault, as shown in Fig. 4.11, no commutation failures were observed in the 0–60° fault angle interval with the new filter in place, for any of the chosen filter frequencies. Figs. 4.10 and 4.11 also show, that the unbalanced system condition during these faults, does not alter the principal effect of the new filter.

Likelihood of Failure with Full Inverter Control

To investigate commutation failure in a more realistic setting, multiple simulations were also performed with the full inverter control activated. This implies that as the

control system senses the drop in the inverter bus voltage due to the fault and the resulting increase in the direct current, the extinction angle of the inverter is quickly advanced to compensate for the lost volt-seconds.

The base case results shown in Fig. 4.12 were taken with a constant extinction angle setting of 22° . The ESCR was 3.0 at the inverter terminal bus and ac system parameters were chosen to suppress the bus voltage by about 30% during faults (base case). The other test cases in Fig. 4.12 again represent more severe conditions for producing commutation failures. The results of the four tests shown are presented in a similar fashion as in Fig. 4.9, comparing the likelihood of failure with and without the new filter, which was tuned at three different frequencies as before. Again, the fault angle is associated with the commutation in a particular (arbitrary) valve-pair relative to the time of fault occurrence. The fault angle was varied in 5° increments between simulation runs.

Comparison of the first two cases (base case and $\text{ESCR} = 2.0$) shows that the new filter virtually eliminates commutation failure, when converter control is in operation, regardless of which of the three filter frequencies is used. In the last two cases, however, the likelihood of failure is reduced by a factor of four, with filters 1 and 2 connected and tuned at 120 Hz and 140 Hz, respectively, whereas filter 3, which was tuned at 160 Hz, still eliminates all failures in the particular valve pair under observation.

Fig. 4.12 illustrates the occurrence of commutation failures due to a three-phase fault applied at different time instances, corresponding to a variable fault angle. Additional simulation runs were performed with different types of faults applied. Thus, Figs. 4.13 and 4.14 show the commutation failure record for a line-to-line and a single-phase to ground faults, respectively. As when the inverter controls were held fixed, a reduction in the likelihood of failure is observed when these fault types are applied. In particular, with a single-phase fault, no failures at all were recorded when the new filter was in place.

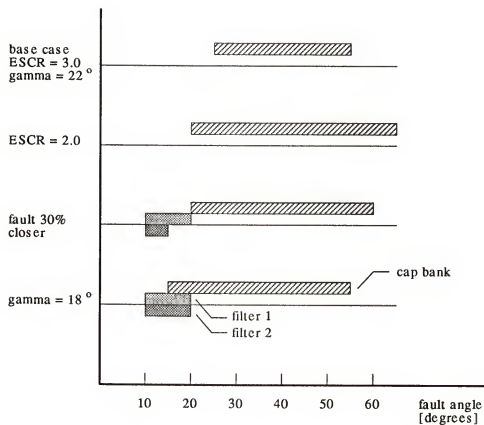


Fig. 4.12 Commutation failures in a specified valve-pair with full inverter control and three-phase fault.

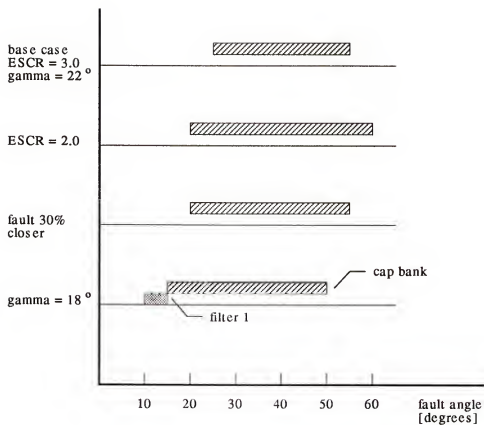


Fig. 4.13 Commutation failures in a specified valve-pair with full inverter control and line-to-line fault.

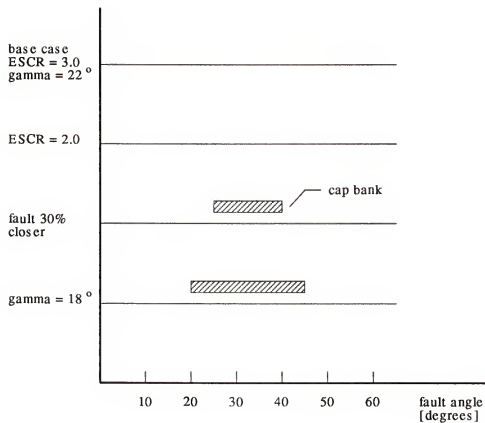


Fig. 4.14 Commutation failures in a specified valve-pair with full inverter control and single-phase fault.

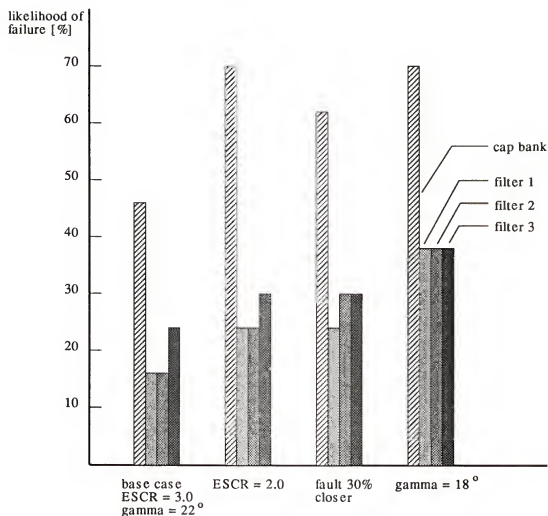


Fig. 4.15 Likelihood of failure in a specified valve pair with fixed inverter control, due to a three-phase fault.

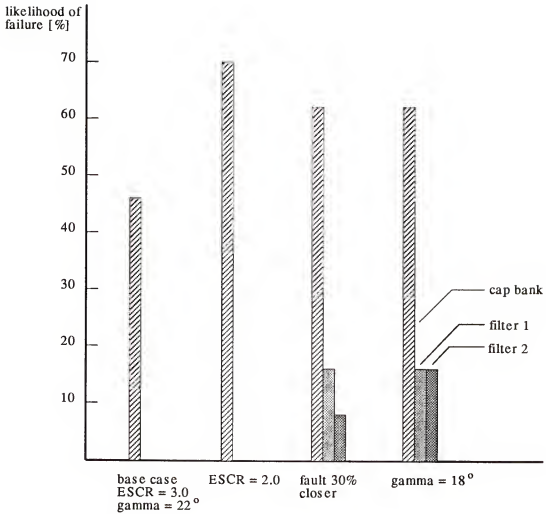


Fig. 4.16 Likelihood of failure in a specified valve pair with full inverter control, due to a three-phase fault.

In summary, the likelihood of commutation failure in the inverter, as defined earlier in this section, due to a three-phase fault, is illustrated in Figs. 4.15 and 4.16, with fixed inverter controls and full controls, respectively. These are essentially the same results as depicted in Figs. 4.9 and 4.12, presented in a different manner, offering an enhanced visual impact of the effects of the new filter. Thus, Fig. 4.15 shows that the likelihood of failure is reduced on the average around 50%, for the given valve-pair, in the specified fault angle interval, with fixed inverter controls. Whereas, with full controls, the likelihood of failure is in some cases drastically reduced and in other cases eliminated altogether.

In the simulation model, the inverter bus voltage is measured through a twelve-pulse diode rectifier, in order to reduce the need for heavy filtering with the associated long time constants. This provides the inverter controls with an effective voltage feedback for the predictive type firing angle control. No attempt was made in this study to optimize the inverter controls, or to coordinate the action of the controls and the new filter, for prevention of commutation failure. It would therefore seem reasonable that the results observed here could be even further improved by optimal tuning of these elements.

Simulation of System Restart after Fault

Two-terminal hvdc links are typically operated in a constant power transmission mode during normal operation. When a fault occurs in the system, causing the ac voltage on either side of the dc link to drop temporarily, a preventive control action is initiated in order to protect the converters from excessive current demands and to prevent a major system outage. During the recovery period, when the fault has cleared and the system is brought back to normal operation, the inverter station may experience high reactive power demands when trying to provide the normal rated current. This may further aggravate the

low-voltage condition, especially in weak ac systems, and may actually prevent recovery from the fault by causing a complete voltage collapse.

In another scenario, if the inverter bus voltage drops due to a fault, the direct current increases momentarily, or until the rectifier controller has reacted to increase the valve gating angle and reduced the rectifier terminal voltage. If a commutation failure results in the inverter due to the disturbance, the inverter terminal looks basically short-circuited as seen from the rectifier side and an inrush of direct current will result into the inverter terminal. Also, the capacitive charge on the dc line and the harmonic filters connected on the dc side of each terminal all add to the current surge.

During the restart period, as the current order is gradually brought back to 100% setting, the inverter is again prone to experience commutation failure, especially if the fault clears soon after it occurred and the restart is initiated promptly, since the transient distortion on the inverter bus voltage may last for several cycles. The rate at which the current order is increased, during the restart phase, is also important.

The problems described above can be remedied, by using a voltage dependent current limit (VDCL). This is a modification of the basic control characteristics for the two-terminal system shown in Fig. 2.16, by reducing the current set-point at the rectifier side, as the direct voltage decreases. Typically, the current order is lowered to around 25–30% of the nominal current setting, which reduces the reactive power demands of the dc system under low voltage conditions, and thus allows a smoother recovery from faults and other severe disturbances. The modified control characteristics for the two-terminal system, including the VDCL, are shown in Fig. 4.17.

Since the proposed new filter tends to increase the higher-order harmonic content on the inverter bus voltage and could therefore possibly aggravate the voltage distortion following a fault, additional simulation tests were performed to compare the performance

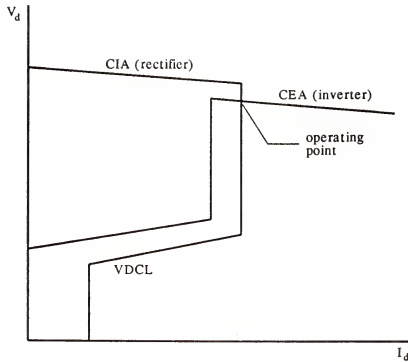
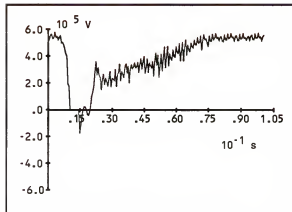
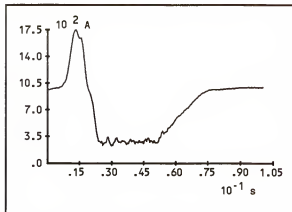


Fig. 4.17 Control characteristics with voltage dependent current limit (VDCL).

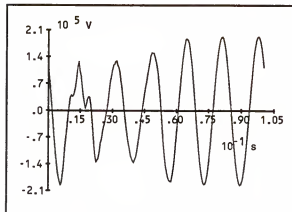
of the filter to that of the straight capacitor bank during the restart interval. The results of these tests are shown in Figs. 4.18 and 4.19, respectively for the capacitor bank and the new filter. For this test, the system parameters were adjusted such that the effective short-circuit ratio at the inverter bus was 2.0, representing a weak system, and the inverter extinction angle was 18° . This represents a somewhat more severe fault condition than illustrated previously, combining two out of four test cases as illustrated for example in Fig. 4.9. The fault was applied for approximately 3 cycles, starting at 5.3 ms simulation time. The severe fault condition resulted in commutation failure immediately following the fault for both system configurations, i.e. with straight capacitor and with new filter



(a)

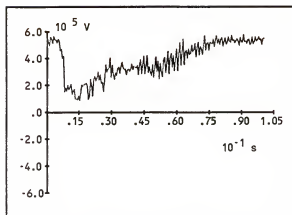


(b)

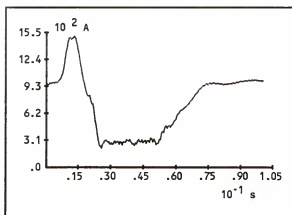


(c)

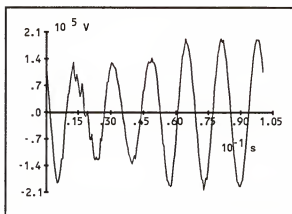
Fig. 4.18 Transient fault response of system with straight capacitor bank during restart; inverter direct voltage (a), direct current (b), inverter bus ac voltage, phase a (c).



(a)



(b)



(c)

Fig. 4.19 Transient fault response of system with new filter during restart; inverter direct voltage (a), direct current (b), inverter bus ac voltage, phase a (c).

installed, as shown in Figs. 4.18 and 4.19, although the filter case fares somewhat better. During the restart period, the increased higher-frequency harmonics due to the filter are manifested in the ac voltage waveform. This however, does not affect the restart process, as no further commutation failures are observed in either case.

CHAPTER 5

CONCLUSION

This investigation establishes a strong relationship between the occurrence of commutation failure in hvdc inverters and the frequency spectrum of the adjoining ac network. It has demonstrated that significant reduction in the probability of failure may be possible by raising the frequency of the dominant low-frequency mode of oscillation. This was demonstrated for a specific test system over a range of critical parameters.

The frequency spectrum of the ac system is closely related to the transient fault response of the inverter bus voltage. When relatively moderate fault disturbances are considered, the transient response of the ac system is largely determined by the characteristic modes or eigenvalues of the linearized system. In this study it has been shown, that the dominant modes can have a major impact on the likelihood of commutation failure in the inverter bridge. By increasing the frequency of the dominant oscillatory mode, the average commutation voltage during the fault period can be increased significantly, which has the effect of reducing the likelihood of commutation failure.

By analysing the sensitivity of the dominant oscillatory mode to the sizes of various parameters in the ac network that connects to the inverter station, it was found that the capacitor bank, which is normally installed for reactive power compensation at the inverter bus, has a crucial effect on the frequency spectrum of the system. The frequency of the dominant mode can be increased by replacing the capacitor bank with a single

tuned filter, similar to the harmonic filters, but tuned at around 120–160 Hz and supplying same amount of VARs at 60 Hz as the capacitor bank. The frequency characteristics of the filter can be adjusted such that the voltage drop due to the fault is minimized during the commutation period.

To evaluate the benefits of the new filter over the straight capacitor bank, in terms of reduced likelihood of commutation failures, an optimization procedure was developed in order to find a best set of parameters for a particular type of filter. A cost function was defined, that measures the voltage excursion on the inverter bus during a fault. Numerical evaluation of the cost function shows, that the new filter offers a reduction in “cost” in the range of 30–40%, when measured over a specified fault angle range. In order to verify this cost reduction in terms of smaller likelihood of commutation failures, extensive simulations were performed, using a two-terminal hvdc system configuration with a weak ac system connected at the inverter terminal. Commutation failures in the inverter were induced, by applying various types of faults at a remote bus in the ac system connected to the inverter terminal.

Clearly this phenomenon needs further study and evaluation in other systems with more types of disturbances, before putting the idea into practice. The specific filter design also needs further scrutiny, as there are many possible circuits that will shift the low-frequency spectrum of the network. Future work should also include the coordination of the inverter control system response with the transient effects of the filter, in order to optimize the benefit. This is particularly important, because, even if the filter fails to prevent a failure, it will probably delay the failure until subsequent valve commutations, which gives the control system additional time to react.

There are a number of other practical aspects which have not been considered in this study. One particular area of concern is the possible negative effects of raising the

low-frequency spectrum of the system. An increased level of higher frequency harmonics was observed in the simulations, with the new filter in place. This possibly could lead to network resonances or transient overvoltages, which could in turn affect ratings of harmonic filters and other equipment. On the positive side, however, the designer of the proposed new filter would have a relatively wide range of frequencies to select from, without severely degrading its performance, since the performance of the filter is relatively insensitive to the filter tuning within a certain frequency range. The particular frequency is not critical; it is only necessary to sufficiently raise the volt-seconds available during commutation. Therefore, to some extent, the filter can be designed to avoid particular troublesome frequencies in the spectrum.

Another area of concern is how effective will the new filter be over a wide range operating conditions. Indeed, there will be many cases of severe faults, in which the fundamental voltage drop is so large that the filter is rendered ineffective and commutation failure will probably occur. In this study with the single tuned filter proposed here, it was observed that it generally becomes ineffective for faults greater than about 40–45%. Also, it is possible that the ac voltage waveform may be severely distorted prior to a fault, and the combined interaction could reduce the effectiveness of the proposed filter. Although it appears that raising the low-frequency spectrum of the ac system should be generally beneficial in reducing commutation failures, independent of the type of disturbance, there is certainly a need for further studies to clarify some of these practical issues.

The costs and benefits of the proposed approach also need to be examined. Reduction in commutation failures in inverters connected to weak ac networks could offer substantial benefits, particularly in multiterminal hvdc systems. In general, this should improve the overall transient performance of the system. It may allow the use of smaller smoothing reactors and lower inverter control angles, than would otherwise be required for low

short-circuit-ratio connections. It may also reduce the effective recovery time for typical fault conditions. On the other hand, the costs appear to be minimal. The present study has shown that the simple single-tuned filter proposed will probably be as good as other more complex topologies. Therefore, the additional cost to the system could only amount to a single inductance per phase, of similar size and cost to those used in conventional harmonic filters.

APPENDIX A

A SAMPLE EMTP DATAFILE FOR SIMULATION
OF A TWO-TERMINAL 12-PULSE HVDC SYSTEM

```

BEGIN NEW DATA CASE
C
C      Twelve pulse, two terminal system.
C      Digital PFC-type control.
C
ABSOLUTE TACS DIMENSIONS
      10      20      20      35      120      2000      180      170
C
      5.0E-5  1.0E-1
      1      1      0      0      0      -1      1      2
      1      1000
C
C      TACS definitions follow. Note: variable TIMEX is the system
C      supplied simulation time in seconds.
C
TACS HYBRID
C
88GAIN      = 30.0
88XLR1      = 25.0
88XLI1      = 15.0
88WR11      = 0.62
C 88GAMREF  = 22.0
88GAMREF    = 18.0
88ELLN      = 180000.0
88ELL1      = 50000.0
88ELL2      = 380000.0
C 88K        = -1.0
88K         = 5.0
88ALIM1     = -1.0
88ALIM2     = 0.0
88TFL1      = TIMEX .GE. 0.010
88TFL2      = TIMEX .GE. 0.020
88TFL3      = TIMEX .GE. 0.052
C
C      Measured dc voltage
C
90VPR1
90VP11
C
C      Measured dc current
C
91IDR1
91IDI1
C
C      Measured ac bus voltage
C
90V DPR1
90VDMR1
88ER1      = 300.0*(VDPR1-VDMR1)

```

```

C
88ELR1  = 280000.0
C
88ELLR1 = ELR1*(1.0-TFL1)+ER1*TFL1
C
90VDPI1
90VDMI1
88EI1   = 300.0*(VDPI1-VDMI1)
C
88ELI1  = 185000.0
C
88ELLM  = ELI1*(1.0-TFL1)+EI1*TFL1
C
88VFL   = ELLM .LT. ELLN
88ELLT  = ELLM*(1.0-TFL3)+(ELLM+K*(ELLM-ELLN)*VFL)*TFL3
OELL11  +ELLT                                ELL1  ELL2
C
90GENAR1
90GENBR1
88GNBAR1 = GENBR1-GENAR1
90GENAI1
90GENBI1
88GNBAI1 = GENBI1-GENAI1
C
90TRFAR1
90TRFBR1
88TFBAR1 = TRFBR1-TRFAR1
90TRFAI1
90TRFBI1
90TRFCI1
88TFBAI1 = TRFBI1-TRFAI1
C
C      Determin alpha max
C
88FXXI1  = 2.*XLI1*IDI1*WRI1/ELLI1-COS(GAMREF*PI/180.)
C
OFXI1    +FXXI1                                ALIM1 ALIM2
88AMAXI1 = 180./PI*ACOS(FXI1)
C
88ALMXR1 = 90.
88ALMXI1 = 140.0*(1.0-TFL1)+AMAXI1*TFL1
C
C      Determin alpha min
C
88ALMNR1 = 6.
88ALMNI1 = 90.
C
C      Calculate dc voltage and set current reference
C

```

```

88VR1      = 1.9099*(1.12*ELLR1*COS(ALPR1*PI/180.))-XLR1*IDR1)
88VI1      = -1.9099*(1.59*ELLI1*COS(ALPI1*PI/180.))-XLI1*IDI1)
C
88IREFR1   = 1000.0
88IREFI1   = 850.0
C
C          Determine ac phase lag.
C
88TGNR1    = GNBAR1 .GT. 0.0
88TTFR1    = TFBAR1 .GT. 0.0
88TPR1     = 360.*TGNR1*DELTAT
88TNR1     = -360.*TTFR1*DELTAT
88RSPR1    = .NOT. TGNR1
88RSNR1    = .NOT. TTFR1
88SMPPR1   = TTFR1*(1.0-TFL3)
88SMPNR1   = TGNR1*(1.0-TFL3)
C
88PHPR1 65+TPR1                                0.0RSPR1 TTFR1
88PHAPR162+PHPR1                                SMPPR1
C
88PHNR1 65+TNR1                                0.0RSNR1 TGNR1
88PHANR162+PHNR1                                SMPNR1
C
88PHASR1 = PHAPR1+PHANR1
C
88TGNI1   = GNBAI1 .GT. 0.0
88TTFI1   = TFBAI1 .GT. 0.0
88TPI1    = 360.*TGNI1*DELTAT
88TNI1    = -360.*TTFI1*DELTAT
88RSP11   = .NOT. TGNI1
88RSN11   = .NOT. TTFI1
88SMPP11  = TTFI1*(1.0-TFL3)
88SMPN11  = TGNI1*(1.0-TFL3)
C
88PHPI1 65+TPI1                                0.0RSP11 TTFI1
88PHAPI162+PHPI1                                SMPP11
C
88PHNI1 65+TNI1                                0.0RSN11 TGNI1
88PHANI162+PHNI1                                SMPN11
C
88PHASI1 = PHAPI1+PHANI1
C
C          Control block follows.
C
88ERRR1   = GAIN/IREFR1*(IDR1-IREFR1)*360.*DELTAT
1DALPR1   +ERRR1
1.0       8.33333E-3
1.0       1.66667E-3
C

```

```

88ERR11 = GAIN/IREF11*(ID11-IREF11)*360.*DELTAT
1DALP11 +ERR11
1.0      8.33333E-3
1.0      1.66667E-3
C
C      Accumulator/counter follows
C
88TMPR1 65+DALPR1                                HOLDR1
88TMP11 65+DALP11                                HOLD11
C
C      Limiter follows
C
0ALPR1  +TMPR1                                ALMNR1ALMXR1
0ALP11  +TMP11                                ALMNI1ALMXI1
C
C      Mode shift logic
C
88IF1R1 = ((ALPR1 .LE. ALMNR1) .AND. (ERRR1 .LE. 0))
88IF2R1 = ((ALPR1 .GE. ALMXR1) .AND. (ERRR1 .GE. 0))
88HOLDR1 = IF1R1 .OR. IF2R1
C
88IF1I1 = ((ALP11 .LE. ALMNI1) .AND. (ERR11 .LE. 0))
88IF2I1 = ((ALP11 .GE. ALMXI1) .AND. (ERR11 .GE. 0))
88HOLDI1 = IF1I1 .OR. IF2I1
C
C      SEQ6 is a system supplied function which converts a given
C      value (K * X) to X, for 0 < X < 7, X = INTEGER, K = INTEGER
C      or REAL, real will be rounded.
C      Example: arguments: -1 0 1 2 3 4 5 6 7 8 9...
C                   result   5 6 1 2 3 4 5 6 1 2 3...
C
88FIRYR1 = SEQ6(TIMEX * 360. - ALPR1 / 60. - PHASR1 + 1.0)
C
98VL1YR1 = FIRYR1 .EQ. 5
98VL2YR1 = FIRYR1 .EQ. 6
98VL3YR1 = FIRYR1 .EQ. 1
98VL4YR1 = FIRYR1 .EQ. 2
98VL5YR1 = FIRYR1 .EQ. 3
98VL6YR1 = FIRYR1 .EQ. 4
C
88FIRD1 = SEQ6(TIMEX * 360. - ALPR1 / 60. - PHASR1 + 0.5)
C
98VL1DR1 = FIRD1 .EQ. 5
98VL2DR1 = FIRD1 .EQ. 6
98VL3DR1 = FIRD1 .EQ. 1
98VL4DR1 = FIRD1 .EQ. 2
98VL5DR1 = FIRD1 .EQ. 3
98VL6DR1 = FIRD1 .EQ. 4
C

```

88FIRY11 = SEQ6(TIMEX * 360. - ALP11 / 60. - PHAS11 + 3.0)

C

98VL1Y11 = FIRY11 .EQ. 1

98VL2Y11 = FIRY11 .EQ. 2

98VL3Y11 = FIRY11 .EQ. 3

98VL4Y11 = FIRY11 .EQ. 4

98VL5Y11 = FIRY11 .EQ. 5

98VL6Y11 = FIRY11 .EQ. 6

C

88FIRDI1 = SEQ6(TIMEX * 360. - ALP11 / 60. - PHAS11 + 2.5)

C

98VL1DI1 = FIRDI1 .EQ. 1

98VL2DI1 = FIRDI1 .EQ. 2

98VL3DI1 = FIRDI1 .EQ. 3

98VL4DI1 = FIRDI1 .EQ. 4

98VL5DI1 = FIRDI1 .EQ. 5

98VL6DI1 = FIRDI1 .EQ. 6

C

C TACS output variables

C

33VP11 IDR1 ALP11 TRFA11TRFB11TRFC11

C

C TACS initial conditions

C

77TMPR1 6.0

77TMP11 135.0

C

BLANK CARD TERMINATING TACS DEFINITIONS

C

C Dc Line #1.

C

IDR1	LNR1	0.0	60.0	0.0
------	------	-----	------	-----

LNR1	BUS17	12.0	860.0	0.0
------	-------	------	-------	-----

BUS17	ID11	0.0	60.0	0.0
-------	------	-----	------	-----

C

C Eleventh-harmonic filters.

C

TRFAR1	1.0	50.0	1.163
--------	-----	------	-------

TRFBR1	1.0	50.0	1.163
--------	-----	------	-------

TRFCR1	1.0	50.0	1.163
--------	-----	------	-------

C

TRFA11	1.0	50.0	1.163
--------	-----	------	-------

TRFB11	1.0	50.0	1.163
--------	-----	------	-------

TRFC11	1.0	50.0	1.163
--------	-----	------	-------

C

C Thirteenth-harmonic filters.

C

TRFAR1	1.0	53.3	0.778
--------	-----	------	-------

TRFBR1	1.0	53.3	0.778
--------	-----	------	-------

TRFCR1	1.0	53.3	0.778
--------	-----	------	-------

C

TRFAI1	1.0	53.3	0.778
TRFBI1	1.0	53.3	0.778
TRFCI1	1.0	53.3	0.778

C

C High-pass filters.

C

TRFAR1HPAR1	166.0	0.0	0.0
TRFBR1HPBR1	166.0	0.0	0.0
TRFCR1HPCR1	166.0	0.0	0.0
TRFAR1HPAR1	0.0	9.0	0.0
TRFBR1HPBR1	0.0	9.0	0.0
TRFCR1HPCR1	0.0	9.0	0.0
HPAR1	0.0	0.0	1.504
HPBR1	0.0	0.0	1.504
HPCR1	0.0	0.0	1.504

C

TRFAI1HPAI1	166.0	0.0	0.0
TRFBI1HPBI1	166.0	0.0	0.0
TRFCI1HPCI1	166.0	0.0	0.0
TRFAI1HPAI1	0.0	9.0	0.0
TRFBI1HPBI1	0.0	9.0	0.0
TRFCI1HPCI1	0.0	9.0	0.0
HPAI1	0.0	0.0	1.504
HPBI1	0.0	0.0	1.504
HPCI1	0.0	0.0	1.504

C

C Local load

C

TRFAI1	100.0	88.0	0.0
TRFBI1	100.0	88.0	0.0
TRFCI1	100.0	88.0	0.0

C

C Capacitor bank

C

TRFAR1	0.5	0.0	3.0
TRFBR1	0.5	0.0	3.0
TRFCR1	0.5	0.0	3.0

C

TRFAI1	0.5	0.0	17.6
TRFBI1	0.5	0.0	17.6
TRFCI1	0.5	0.0	17.6

C

C Generator reactances.

C

GENAR1ACAR1	29.6	0.0	0.0
GENBR1ACBR1	29.6	0.0	0.0
GENCR1ACCR1	29.6	0.0	0.0

GENAR1ACAR1	0.0	55.6	0.0
GENBR1ACBR1	0.0	55.6	0.0
GENCR1ACCR1	0.0	55.6	0.0
ACAR1 TRFAR1	0.0	111.1	0.0
ACBR1 TRFBR1	0.0	111.1	0.0
ACCR1 TRFCR1	0.0	111.1	0.0
C			
GENA11ACAI1	14.4	0.0	0.0
GENB11ACBI1	14.4	0.0	0.0
GENC11ACCI1	14.4	0.0	0.0
GENA11ACAI1	0.0	26.9	0.0
GENB11ACBI1	0.0	26.9	0.0
GENC11ACCI1	0.0	26.9	0.0
ACA11 TRFA11	0.0	54.0	0.0
ACB11 TRFB11	0.0	54.0	0.0
ACC11 TRFC11	0.0	54.0	0.0
C			
C GENA11ACAI1	19.4	0.0	0.0
C GENB11ACBI1	19.4	0.0	0.0
C GENC11ACCI1	19.4	0.0	0.0
C GENA11ACAI1	0.0	36.3	0.0
C GENB11ACBI1	0.0	36.3	0.0
C GENC11ACCI1	0.0	36.3	0.0
C ACA11 TRFA11	0.0	73.0	0.0
C ACB11 TRFB11	0.0	73.0	0.0
C ACC11 TRFC11	0.0	73.0	0.0
C			
C AC line to remote load bus LB #1			
C			
TRFA11LB1A11	12.0	195.0	0.0
TRFB11LB1B11	12.0	195.0	0.0
TRFC11LB1C11	12.0	195.0	0.0
C			
C TRFA11LB1A11	8.4	136.5	0.0
C TRFB11LB1B11	8.4	136.5	0.0
C TRFC11LB1C11	8.4	136.5	0.0
C			
C Remote load			
C			
LB1A11	325.0	284.0	0.0
LB1B11	325.0	284.0	0.0
LB1C11	325.0	284.0	0.0
C			
C Capacitor bank at remote load bus			
C			
LB1A11	0.5	0.0	4.0
LB1B11	0.5	0.0	4.0
LB1C11	0.5	0.0	4.0
C			

C R-C snubbers for main valves follow

C

BSAYR1VPAYR1	3500.0	0.0	0.05
BSBYR1VPBYR1	3500.0	0.0	0.05
BSCYR1VPCYR1	3500.0	0.0	0.05
VMAYR1BSAYR1	3500.0	0.0	0.05
VMBYR1BSBYR1	3500.0	0.0	0.05
VMCYR1BSCYR1	3500.0	0.0	0.05

C

BSADR1VPADR1	3500.0	0.0	0.05
BSBDR1VPBDR1	3500.0	0.0	0.05
BSCDR1VPCDR1	3500.0	0.0	0.05
VMADR1BSADR1	3500.0	0.0	0.05
VMBDR1BSBDR1	3500.0	0.0	0.05
VMCDR1BSCDR1	3500.0	0.0	0.05

C

BSAYI1VPAYI1	3500.0	0.0	0.05
BSBYI1VPBYI1	3500.0	0.0	0.05
BSCYI1VPCYI1	3500.0	0.0	0.05
VMAYI1BSAYI1	3500.0	0.0	0.05
VMBYI1BSBYI1	3500.0	0.0	0.05
VMCYI1BSCYI1	3500.0	0.0	0.05

C

BSADI1VPADI1	3500.0	0.0	0.05
BSBDI1VPBDI1	3500.0	0.0	0.05
BSCDI1VPCDI1	3500.0	0.0	0.05
VMADI1BSADI1	3500.0	0.0	0.05
VMBDI1BSBDI1	3500.0	0.0	0.05
VMCDI1BSCDI1	3500.0	0.0	0.05

C

C Valve series resistance.

C

VPAYR1VPR1	0.1E-3	0.0	0.0
VPBYR1VPR1	0.1E-3	0.0	0.0
VPCYR1VPR1	0.1E-3	0.0	0.0
VMAYR1VCR1	0.1E-3	0.0	0.0
VMBYR1VCR1	0.1E-3	0.0	0.0
VMCYR1VCR1	0.1E-3	0.0	0.0

C

VPADR1VCR1	0.1E-3	0.0	0.0
VPBDR1VCR1	0.1E-3	0.0	0.0
VPCDR1VCR1	0.1E-3	0.0	0.0
VMADR1	0.1E-3	0.0	0.0
VMBDR1	0.1E-3	0.0	0.0
VMCDR1	0.1E-3	0.0	0.0

C

VPAYI1	0.1E-3	0.0	0.0
VPBYI1	0.1E-3	0.0	0.0
VPCYI1	0.1E-3	0.0	0.0

VMAY11VC11	0.1E-3	0.0	0.0
VMBY11VC11	0.1E-3	0.0	0.0
VMCY11VC11	0.1E-3	0.0	0.0

C

VPAD11VC11	0.1E-3	0.0	0.0
VPBD11VC11	0.1E-3	0.0	0.0
VPCD11VC11	0.1E-3	0.0	0.0
VMAD11VP11	0.1E-3	0.0	0.0
VMBD11VP11	0.1E-3	0.0	0.0
VMCD11VP11	0.1E-3	0.0	0.0

C

C Wye-wye transformer data, Rectifier #1.

C

TRANSFORMER		TAYR1
9999		
1TRFAR1	0.0	76.5 1.550
2BSAYR1NEUYR1	0.0	31.8 1.0
TRANSFORMER TAYR1		TBYR1
1TRFBR1		
2BSBYR1NEUYR1		
TRANSFORMER TAYR1		TCYR1
1TRFCR1		
2BSCYR1NEUYR1		

C

C Wye-delta transformer data, Rectifier #1.

C

TRANSFORMER		TADR1
9999		
1TRFAR1	0.0	76.5 0.895
2BSADR1BSBDR1	0.0	95.5 1.0
TRANSFORMER TADR1		TBDR1
1TRFBR1		
2BSBDR1BSCDR1		
TRANSFORMER TADR1		TCDR1
1TRFCR1		
2BSCDR1BSADR1		

C

C Wye-wye transformer data, Inverter #1.

C

TRANSFORMER		TAYI1
9999		
1TRFAI1	0.0	20.6 1.09
2BSAYI1NEUYI1	0.0	17.3 1.0
TRANSFORMER TAYI1		TBYI1
1TRFBI1		
2BSBYI1NEUYI1		
TRANSFORMER TAYI1		TCYI1
1TRFCI1		
2BSCYI1NEUYI1		

C
C Wye-delta transformer data, Inverter #1.

C
TRANSFORMER TADI1
 9999
1TRFAI1 0.0 20.6 0.63
2BSADI1BSBDI1 0.0 51.9 1.0
TRANSFORMER TADI1 TBDI1
1TRFBI1
2BSBDI1BSCDI1
TRANSFORMER TADI1 TCDI1
1TRFCI1
2BSCDI1BSADI1

C
C Measuring transformer Y-Y, Rectifier #1.

C
TRANSFORMER TMAYR1
 9999
1TRFAR1 0.0 10.6 1000.
2TFAYR1NEYR1 0.0 10.6 1.0
TRANSFORMER TMAYR1 TMBYR1
1TRFBR1
2TFBYR1NEYR1
TRANSFORMER TMAYR1 TMCYR1
1TRFCR1
2TFCYR1NEYR1

C
C Measuring transformer Y-D, Rectifier #1.

C
TRANSFORMER TMADR1
 9999
1TRFAR1 0.0 10.6 575.0
2TFADR1TFBDR1 0.0 10.6 1.0
TRANSFORMER TMADR1 TMBDR1
1TRFBR1
2TFBDR1TFCDR1
TRANSFORMER TMADR1 TMCDR1
1TRFCR1
2TFCDR1TFADR1

C
C Measuring transformer Y-Y, Inverter #1.

C
TRANSFORMER TMAYI1
 9999
1TRFAI1 0.0 10.6 1000.
2TFAYI1NEYI1 0.0 10.6 1.0
TRANSFORMER TMAYI1 TMBYI1
1TRFBI1
2TFBYI1NEYI1

```

TRANSFORMER TMAY11          TMCY11
1TRFC11
2TFCY11NEY11
C
C      Measuring transformer Y-D, Inverter #1.
C
TRANSFORMER                  TMAD11
      9999
1TRFA11                      0.0 10.6 571.0
2TFAD11TFBD11                0.0 10.6 1.0
TRANSFORMER TMAD11          TMBD11
1TRFB11
2TFBD11TFCD11
TRANSFORMER TMAD11          TMCD11
1TRFC11
2TFCD11TFAD11
C
C      RC dampers for diode measuring bridge.
C
TFAYR1DPAYR1                3500.0 0.0 0.05
TFBYR1DPBYR1                3500.0 0.0 0.05
TFCYR1DPCYR1                3500.0 0.0 0.05
DMAYR1TFAYR1                3500.0 0.0 0.05
DMBYR1TFBYR1                3500.0 0.0 0.05
DMCYR1TFCYR1                3500.0 0.0 0.05
C
TFADR1DPADR1                3500.0 0.0 0.05
TFBDR1DPBDR1                3500.0 0.0 0.05
TFCDR1DPCDR1                3500.0 0.0 0.05
DMADR1TFADR1                3500.0 0.0 0.05
DMBDR1TFBDR1                3500.0 0.0 0.05
DMCDR1TFCDR1                3500.0 0.0 0.05
C
TFAY11DPAY11                3500.0 0.0 0.05
TFBY11DPBY11                3500.0 0.0 0.05
TFCY11DPCY11                3500.0 0.0 0.05
DMAY11TFAY11                3500.0 0.0 0.05
DMBY11TFBY11                3500.0 0.0 0.05
DMCY11TFCY11                3500.0 0.0 0.05
C
TFAD11DPAD11                3500.0 0.0 0.05
TFBD11DPBD11                3500.0 0.0 0.05
TFCD11DPCD11                3500.0 0.0 0.05
DMAD11TFAD11                3500.0 0.0 0.05
DMBD11TFBD11                3500.0 0.0 0.05
DMCD11TFCD11                3500.0 0.0 0.05
C
C      Series resistance for diode rectifier.
C

```

DPAYR1VDDR1	0.1E-3	0.0	0.0
DPBYR1VDDR1	0.1E-3	0.0	0.0
DPCYR1VDDR1	0.1E-3	0.0	0.0
DMAYR1VCDR1	0.1E-3	0.0	0.0
DMBYR1VCDR1	0.1E-3	0.0	0.0
DMCYR1VCDR1	0.1E-3	0.0	0.0
C			
DPADR1VCDR1	0.1E-3	0.0	0.0
DPBDR1VCDR1	0.1E-3	0.0	0.0
DPCDR1VCDR1	0.1E-3	0.0	0.0
DMADR1VDMR1	0.1E-3	0.0	0.0
DMBDR1VDMR1	0.1E-3	0.0	0.0
DMCDR1VDMR1	0.1E-3	0.0	0.0
C			
VDMR1	0.1E-3	0.0	0.0
C			
DPAYI1VDDI1	0.1E-3	0.0	0.0
DPBYI1VDDI1	0.1E-3	0.0	0.0
DPCYI1VDDI1	0.1E-3	0.0	0.0
DMAYI1VCDI1	0.1E-3	0.0	0.0
DMBYI1VCDI1	0.1E-3	0.0	0.0
DMCYI1VCDI1	0.1E-3	0.0	0.0
C			
DPADI1VCDI1	0.1E-3	0.0	0.0
DPBDI1VCDI1	0.1E-3	0.0	0.0
DPCDI1VCDI1	0.1E-3	0.0	0.0
DMADI1VDMI1	0.1E-3	0.0	0.0
DMBDI1VDMI1	0.1E-3	0.0	0.0
DMCDI1VDMI1	0.1E-3	0.0	0.0
C			
VDMI1	0.1E-3	0.0	0.0
C			
C	RC filter for voltage measuring bridge.		
C			
VDDR1 VDMR1	1.0E+4	0.0	0.0
VDDR1 VDPR1	1.0E+4	0.0	0.0
VDPR1 VDMR1	0.0	0.0	0.1
C			
VDDI1 VDMI1	1.0E+4	0.0	0.0
VDDI1 VDPI1	1.0E+4	0.0	0.0
VDPI1 VDMI1	0.0	0.0	0.1
C			
BLANK END OF BRANCH DEFINITIONS			
C			
C	Measuring switches		
C			
VPR1 IDR1		MEASURING	
IDI1 VPI1		MEASURING	
C			

C Fault switches, load bus LB #1

C

LB1A11	0.1555	0.510
LB1B11	0.1555	0.510
LB1C11	0.1555	0.510

C

C Twelve-pulse diode rectifier for bus voltage measurement.

C

11TFAYR1DPAYR1
11TFBYR1DPBYR1
11TFCYR1DPCYR1
11DMAYR1TFAYR1
11DMBYR1TFBYR1
11DMCYR1TFCYR1

C

11TFADR1DPADR1
11TFBDR1DPBDR1
11TFCDR1DPCDR1
11DMADR1TFADR1
11DMBDR1TFBDR1
11DMCDR1TFCDR1

C

11TFAYI1DPAYI1
11TFBYI1DPBYI1
11TFCYI1DPCYI1
11DMAYI1TFAYI1
11DMBYI1TFBYI1
11DMCYI1TFCYI1

C

11TFADI1DPADI1
11TFBDI1DPBDI1
11TFCDI1DPCDI1
11DMADI1TFADI1
11DMBDI1TFBDI1
11DMCDI1TFCDI1

C

C Converter valves

C

11BSAYR1VPAYR1	CLOSED	VL1YR1
11BSBYR1VPBYR1		VL3YR1
11BSCYR1VPCYR1		VL5YR1
11VMAYR1BSAYR1		VL4YR1
11VMBYR1BSBYR1		VL6YR1
11VMCYR1BSCYR1	CLOSED	VL2YR1
11BSADR1VPADR1	CLOSED	VL1DR1
11BSBDR1VPBDR1		VL3DR1
11BSCDR1VPCDR1		VL5DR1
11VMADR1BSADR1		VL4DR1

11VMBDR1BSBDR1		VL6DR1
11VMCDR1BSCDR1	CLOSED	VL2DR1
C		
11BSAY11VPAY11		VL1Y11
11BSBY11VPBY11		VL3Y11
11BSCY11VPCY11	CLOSED	VL5Y11
11VMAY11BSAY11		VL4Y11
11VMBY11BSBY11	CLOSED	VL6Y11
11VMCY11BSCY11		VL2Y11
C		
11BSAD11VPAD11		VL1D11
11BSBD11VPBD11		VL3D11
11BSCD11VPCD11	CLOSED	VL5D11
11VMAD11BSAD11		VL4D11
11VMBD11BSBD11	CLOSED	VL6D11
11VMCD11BSCD11		VL2D11

BLANK END SWITCH CARDS

C

C

AC voltage sources

C

14GENAR1 1	303000.	60.0	60.0	0.0
14GENBR1 1	303000.	60.0	-60.0	0.0
14GENCR1 1	303000.	60.0	180.0	0.0

C

14GENAI1 1	188000.	60.0	60.0	0.0
14GENBI1 1	188000.	60.0	-60.0	0.0
14GENCI1 1	188000.	60.0	180.0	0.0

C

BLANK END OF SOURCE DEFINITIONS

C

C

Initial direct current.

C

3IDR1	LNR1	1000.
3LNR1	BUS17	1000.
3BUS17	ID11	1000.

C

C

Node voltages for plotting

C

BLANK CARD END OF INITIAL CONDITIONS AND PLOT NODES

C

PRINTER PLOT

C

A CHAR: ALPR1

19410. 0. 100. 0.0 65.0TACS ALPR1

C

A CHAR: IDR1

19410. 0. 100.-.6E32.E3TACS IDR1

C

A CHAR: VPI1
19410. 5. 100.-.5E56.E5TACS VP11
C
A CHAR: TRFA11
B CHAR: TRFB11
19410. 5. 100. TACS TRFA11TACS TRFB11
C
A CHAR: TRFC11
19410. 5. 100. TACS TRFC11
C
BLANK CARD ENDING PLOT CARDS
C
BLANK END OF SIMULATION

APPENDIX B

SCHEMATIC DIAGRAMS OF TEST SYSTEM MODEL

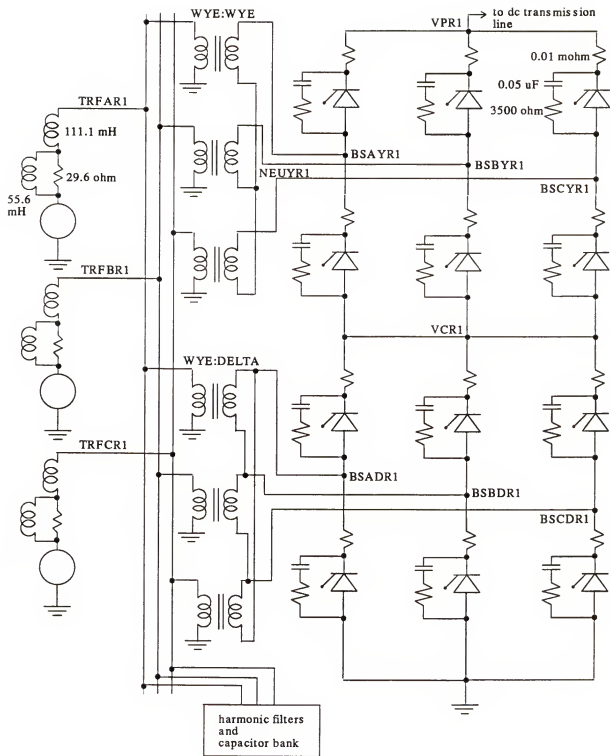


Fig. B.1 Rectifier bridge and adjoining ac network.

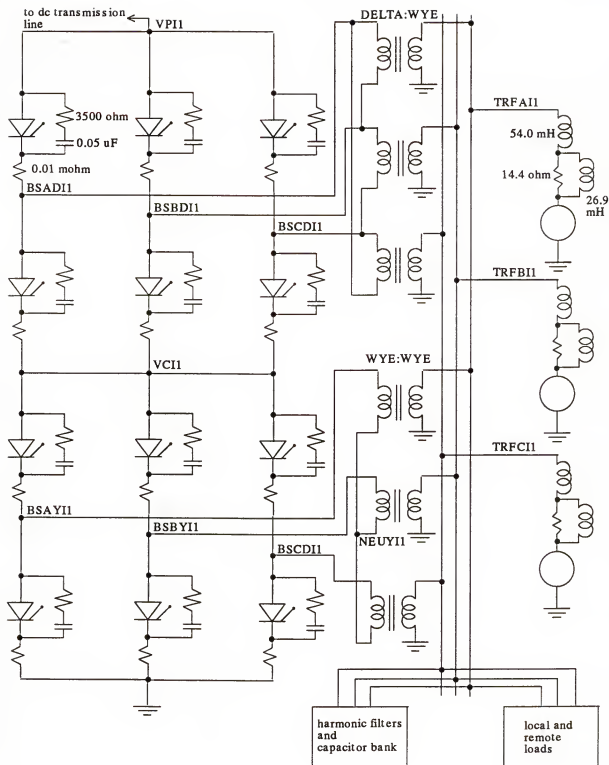


Fig. B.2 Inverter bridge and adjoining ac network.

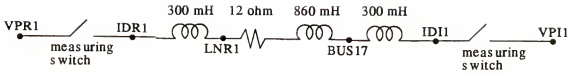


Fig. B.3 Dc transmission line and smoothing reactors.

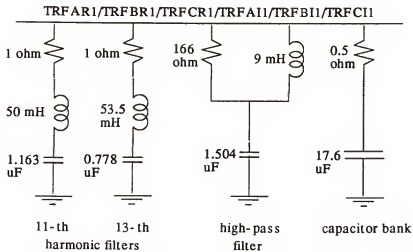


Fig. B.4 Harmonic filters and capacitor banks at rectifier and inverter terminals.

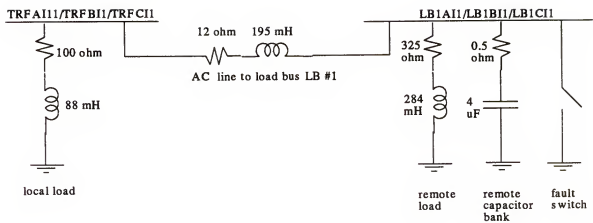


Fig. B.5 Local and remote loads connected to inverter station.

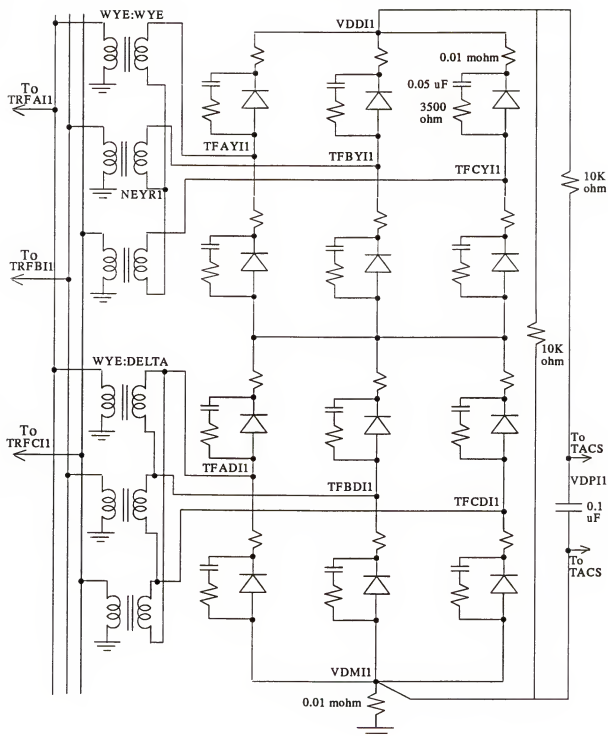


Fig. B.7 Measuring circuit for inverter bus voltage.

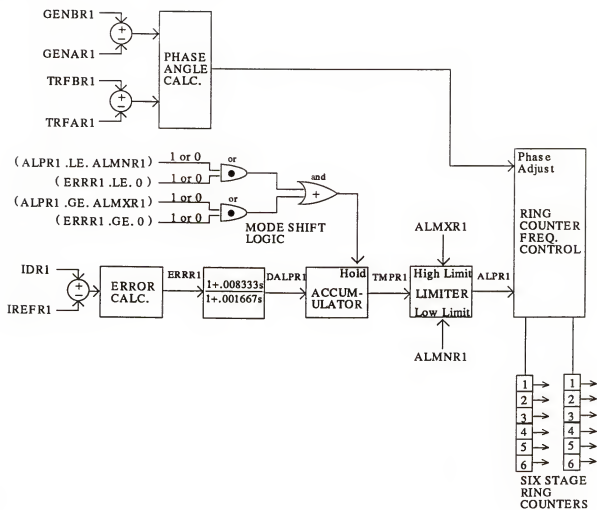


Fig. B.8 Rectifier control circuits.

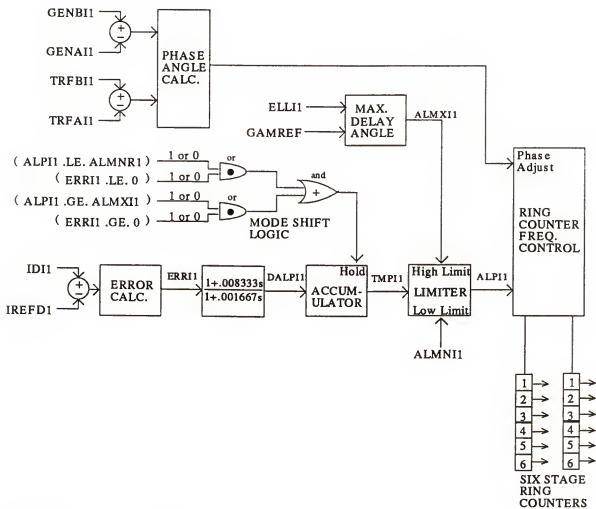


Fig. B.9 Inverter control circuits.

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BIOGRAPHICAL SKETCH

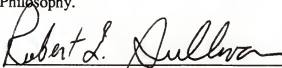
Gudleifur Maris Kristmundsson was born in Hafnarfjörður, Iceland, on March 29, 1949. He received the BSEE degree from the University of Iceland in 1974 and studied automatic control at Lund's Technical College, in Lund, Sweden, in 1974–1975. He was employed as engineer by Landsvirkjun, The National Power Company, Reykjavik, Iceland, in 1975–1982. In 1982 he was awarded a Fulbright Grant and a scholarship from the American-Scandinavian Foundation for graduate studies in the United States. He was admitted to the Graduate School at the University of Florida, where he received the Master of Engineering degree in 1984. He has been enrolled in the Ph.D. program at the University of Florida since 1985.

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Dennis P. Carroll, Chairman
Professor of Electrical Engineering

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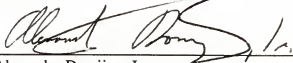
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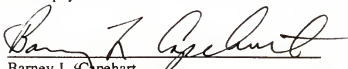
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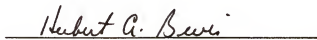
Alexander Domijan, Jr.
Assistant Professor of Electrical Engineering

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Barney L. Capehart
Professor of Industrial and Systems Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May 1989


Dean, College of Engineering

Dean, Graduate School